SRI RAMAKRISHNA
COLLEGE OF ARTS AND SCIENCE
(An Autonomous Institution)
Nava India, Avinashi Road, Coimbatore

Learning Outcomes-Based Curriculum Framework (LOCF)

for

Post Graduate Programme
MSc (Electronics and Communication System)

under

Regulations 2020

For 2020 Admitted Batch onwards

SRI RAMAKRISHNA
COLLEGE OF ARTS AND SCIENCE
(An Autonomous Institution)
Nava India, Avinashi Road, Coimbatore

Scheme of Examination

(For the students admitted during the academic year 2020 - 2021 and onwards)

Under
Choice Based Credit System (CBCS)
& Learning Outcomes-Based Curriculum Framework (LOCF)

POSTGRADUATE PROGRAMMES

Programme: M.Sc Branch: Electronics and Communication System

Course Code	Study Components and Course Title	CIA	Comprehensive Exam		Comprehensive Exam Total	Total	Credit
			Online	Descriptive Theory			
	I SEMESTER						
20MEC101	CORE I – Embedded system and IoT	**40**	**10**	**50**	**60**	**100**	**4**
20MEC102	CORE II –VHDL Programming and Lab	**50**	**-**	**50**	**50**	**100**	**5**
20MEC103	CORE III – Microwave and Radar Navigation System	**40**	**10**	**50**	**60**	**100**	**3**
20MECE01/ 02/03	**DS Elective –I**	**40**	**10**	**50**	**60**	**100**	**4**
20MEC104	CORE – IV Digital Communication and Network Techniques	**40**	**10**	**50**	**60**	**100**	**4**
20MEC105	CORE – V PRACTICAL –I Embedded System Lab	**40**	**-**	**60**	**60**	**100**	**4**

	II SEMESTER						
20MEC201	CORE – VI Arduino Programming and lab	**50**	**-**	**50**	**50**	**100**	**5**
20MEC202	CORE – VII VERILOG Programming	**40**	**10**	**50**	**60**	**100**	**4**
20MEC203	CORE – VIII PRACTICAL –II VERILOG Programming lab	**40**	**-**	**60**	**60**	**100**	**4**
20MEC204	CORE – IX Analysis and Processing of Signals	**40**	**10**	**50**	**60**	**100**	**4**
20MEC205	CORE –X Automotive Embedded Systems	**40**	**10**	**50**	**60**	**100**	**3**
20MECE04/ 05/06	**DS Elective – II**	**40**	**10**	**50**	**60**	**100**	**4**
20MEA01	Mandatory Non-CGPA **AEC** / MACE @				**100**	**100****	**2$**
20MEC206	Mandatory Non-CGPA **(Summer Project-1 /Internship/Teaching Assignment)**	**100**				**100****	**1$**
20VEA01	**Mandatory Non-CGPA Co/Extra CC/VE**	**100**				**100****	**1$**
	III SEMESTER						
20MEC301	CORE – XI Digital Signal Processor	**40**	**10**	**50**	**60**	**100**	**4**
20MEC302	CORE – XII PRACTICAL –III Digital Signal Processor Lab	**40**	**-**	**60**	**60**	**100**	**4**
20MEC303	CORE – XIII Virtual Instrumentation and Lab	**50**	**-**	**50**	**50**	**100**	**5**
20MECI01	IDC / **Generic Elective** – Self-Study paper	**50**	**-**	**50**	**50**	**100**	**4**
20MECE07 /08/09	**DS Elective –III**	**40**	**10**	**50**	**60**	**100**	**4**
20MEA02	Mandatory Non-CGPA **SEC** / MACE @	**100**				**100****	**2$**

	IV SEMESTER						
20MEC401	CORE – XIV IoT using TICC3200 and lab	50	-	50	50	100	5
20MEC402	CORE- XV MEMS and NEMS	40	10	50	60	100	4
20MEC403	**DS Elective –IV** (Self-Study-Research) Research Methodology	40	10	50	60	100	4
20MEC404	CORE –XVI Internship / Capstone Project	120	-	-	80	200	8

$ Extra credit courses

@ Comprehensive Examinations only.

**** Not included in Total Marks and CGPA Calculation.**

@@ MOOC Course -Minimum of 30 Hours from recognized MOOC portal like SWAYAM, Coursera, etc. Assessment with Score/Credit and Certificate is mandatory.

Abstract of

Scheme of Examination

(For the students admitted during the academic year 2020 - 2021 and onwards)

Subject	Papers	Credit	Total credits	marks	Total marks
Core (including Project work & Viva voce)	16	3/4/5/8	6+36+20+8=70	100/200	1700
DS Elective	4	4	16	100	400
IDC / **Generic Elective**	1	4	4	100	100
Mandatory Non-CGPA **AEC** / MACE	1	2	2$	100	100**
Mandatory Non-CGPA **SEC** / MACE	1	2	2$	100	100**
Mandatory Non-CGPA **(Summer Project-1)**	1	1	1$	100	100**
Mandatory Non-CGPA **(Co/Extra Curricular/VE)**	1	1	1$	100	100**
Total			**90 + (6 Extra Credits)**		2200+ (400**)

Note:

- **Two core courses are mandatory in MOOC Portal**
- **Minimum 20 and Maximum 24 Credit/Semester**

List of Elective Papers / DSE (Can choose any one of the paper as electives)		
	Course Code	**Title**
Electives Track -1 (SLET/NET)- / **DSE-I**	20MECE01	Power Electronics and Control Systems
	20MECE02	Fiber Optic communication
	20MECE03	Microprocessor and Microcontrollers
Electives Track -2 (Research) / **DSE-II**	20MECE04	CRYPTOGRAPHY
	20MECE05	Digital CMOS VLSI Design
	20MECE06	ASIC Design
Electives Track -3 (Entrepreneurship & Innovation) / **DSE-III**	20MECE07	Artificial Intelligence for Electronics
	20MECE08	Robotics and Automation
	20MECE09	Digital Image Processing

IDC / **Generic Elective** – Self-Study paper	20MECI01	Fundamentals of Embedded System

Syllabus Coordinator

Dr Thamarai Selvan M

BOS Chairperson

Dr Poornima K

Academic Council – Member Secretary

Dr Jayasheela D

Outline of Learning Outcomes-Based Curriculum Framework (LOCF)

1. Core Course: A course, which should compulsorily be studied by a candidate as a core requirement is termed as a Core course.

2. Elective Course: Generally a course which can be chosen from a pool of courses and which may be very specific or specialized or advanced or supportive to the discipline/subject of study or which provides an extended scope or which enables an exposure to some other discipline/subject/domain or nurtures the candidate's proficiency/skill is called an Elective Course.

2.1 Discipline Specific Elective (DSE) Course: Elective courses may be offered by the **main discipline/subject of study** is referred to as Discipline Specific Elective. The Institute may also offer discipline related Elective courses of interdisciplinary nature (to be offered by main discipline/subject of study).

2.2 Dissertation/Project: An elective course designed to acquire special/advanced knowledge, such as supplement study/support study to a project work, and a candidate studies such a course on his own with an advisory support by a teacher/faculty member is called dissertation/project.

2.3 Generic Elective (GE) Course: An elective course chosen generally from an **unrelated discipline/subject**, with an intention to seek exposure is called a Generic Elective.

P.S.: A core course offered in a discipline/subject may be treated as an elective by other discipline/subject and vice versa and such electives may also be referred to as Generic Elective.

3. Ability Enhancement Courses (AEC): The Ability Enhancement (AE) Courses may be of two kinds: Ability Enhancement Compulsory Courses (AECC) and Skill Enhancement Courses (SEC). "AECC" courses are the courses based upon the content that leads to Knowledge enhancement; i. Environmental Science and ii. English/MIL Communication.

These are mandatory for all disciplines. SEC courses are value-based and/or skill-based and are aimed at providing hands-on-training, competencies, skills, etc.

3.1 Ability Enhancement Compulsory Courses (AECC): Environmental Science, English Communication/ Media and Information Literacy (MIL) Communication.

3.2 Skill Enhancement Courses (SEC): These courses may be chosen from a pool of courses designed to provide value-based and/or skill-based knowledge.

Introducing Research Component in Under-Graduate Courses

Project work/Dissertation is considered as a special course involving application of knowledge in solving / analyzing /exploring a real life situation / difficult problem. A Project/Dissertation work would be of 6 credits. A Project/Dissertation work may be given in lieu of a discipline specific elective paper.

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SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC101	Embedded system and IoT	Core	55	-	-	4	Theory

PREAMBLE / COURSE OBJECTIVE

This course aims at understand the basics architecture of 16-bit microcontrollers. The course helps the students to understand hardware interfacing concepts to connect digital as well as analog sensors while ensuring low power considerations. The reviews and implement the protocols used by microcontroller to communicate with external sensors and actuators in real world. The course helps the students to Study the various Embedded Networking concepts based upon connected MCUs.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals knowledge on Basic Microprocessor and Microcontrollers

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Describe architecture and operation of Microcontroller	Understand
CO2	Review the fundamentals of Microcontroller	Understand
CO3	Apply low power features during designing a model	Remember
CO4	Interface protocol for communicating with external devices	Apply
CO5	Work on embedded networking concepts.	Apply

SYLLABUS

UNIT I Introduction to Embedded Systems — 11 HOURS

Embedded system overview, applications, features and architecture considerations - ROM, RAM, timers, data and address bus, I/O interfacing concepts, memory mapped I/O. CISC Vs RISC design philosophy. Von-Neumann Vs Harvard architecture.

MSP430x5x series block diagram, address space, on-chip peripherals (analog and digital), and Register sets. Instruction set, instruction formats, and various addressing modes of 16-bit microcontroller; MSP430 specifics. Variants of the MSP430 family viz. MSP430x2x, MSP430x4x, MSP430x5x and their targeted applications, Sample embedded system on MSP430 microcontroller.

UNIT II Microcontroller Fundamentals for Basic Programming — 11 HOURS

Memory Mapped Peripherals, programming System registers, I/O pin multiplexing & its relevance, pull up/down registers, GPIO control, Interrupt and Interrupt Programming, Watchdog Timer, System clocks. Need of low power for embedded systems, system clocks and Low power modes.

Low Power aspects of MSP430: low power modes, Active vs Standby current consumption, FRAM vs Flash for low power & reliability.

Case Study: MSP430 based embedded system application bringing up the salient features of GPIO, Watchdog timer, low power, FRAM etc.

Advance Topic: Energy and power consumption estimation for embedded board

UNIT III Timers, PWM and Mixed Signals Processing — 11 HOURS

Timer Basic, Timer & Real Time Clock (RTC), PWM control, Timing generation and measurements, Analog interfacing and data acquisition: ADC and Comparator in MSP430, DMA for data transfer.

Power considerations: Programming for optimal power consumption while using peripherals, Using MSP430 peripheral intelligence in power management.

Case Study: MSP430 based embedded system application using ADC & PWM demonstrating peripheral intelligence. - "Remote Controller of Air Conditioner Using MSP430"

UNIT IV Communication Protocols and Interfacing with External Devices — 11 HOURS

Serial communication basics, Synchronous/Asynchronous interfaces (like UART, USB, SPI, I2C),

Implementing and programming UART, I2C, SPI interface using MSP430, Interfacing external devices.

Case Study: MSP430 based embedded system application using the interface protocols for communication with external devices: A

UNIT V Embedded Networking and Internet of Things — 11 HOURS

IoT overview and architecture, Overview of wireless sensor networks and design examples.

Various wireless connectivity: NFC, ZigBee, Bluetooth, Bluetooth Low Energy, Wi-Fi.

Adding Wi-Fi capability to the Microcontroller, Embedded Wi-Fi, User APIs for Wireless and Networking applications. Building IoT applications using CC32xx user API: connecting sensor devices

Case Study: MSP430 based Embedded Networking Application: "Implementing Wi-Fi Connectivity in a Smart Electric meter

TEXT BOOKS

A. M. Alagappan, K. Hariharan, Raghav ankur and KG. Srinivasa "Embedded System Design using MSP430", Texas instruments 2017.

B. Steven F Barrett, Daniel J Pack. " Microcontroller Programming and Interfacing Texas Instruments MSP 430" Morgan & Claypool Publishers, 2011

C. John Davies, "MSP Microcontroller Basics", Newnes First Edition. 2008

REFERENCE BOOK

A. MSP430 Microcontroller Projects – Dr. C. P. Ravikumar .

WEB RESOURCES

A. http://www.ti.com/sc/data/msp/databook/chp1.pdf

B. https://www.ti.com/product/MSP430F149

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	-	-	S	S	-	-	L	-	S
CO2	S	-	-	S	M	-	-	S	-	S
CO3	M	-	-	L	S	-	-	S	-	S
CO4	S	-	-	S	S	S	-	S	-	S
CO5	S	-	-	S	S	S	-	S	-	S

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Prepared by
Ms Indira S

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC102	VHDL Programming and Lab	Core	35	-	40	5	Integrated (Theory and Practical)

PREAMBLE / COURSE OBJECTIVE

To enable the students to understand the basic concept of MOS technology and its fabrications and VHDL language. Understanding a three style of modeling such as Data flow, Behavioral, Structural in detail with elements and syntax as well as how it works under simulation and synthesis. To understand the various elements, operators, programming styles and applications of VHDL programming.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals knowledge on basic Digital Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / Skill Development

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Define and List out the different types of terminologies used in VHDL Programming	Remember
CO2	Create hardware models with declaration procedures	Understand
CO3	Develop a model with data object and data types.	Apply
CO4	Design a digital circuit using operators.	Apply
CO5	Design a circuit using various modeling styles.	Apply

SYLLABUS

UNIT I Introduction to VHDL — 7 HOURS

Basic terminology – Design flow – VHDL objects – Entity declarations – Architectural body – Process declarations – Configuration – Functions – Procedures – Package declaration and Package body.

Practical: 1. Verification of logic gates with test bench.
2. Four bit full adder and Subtractor in single module with test bench. — **8 HOURS**

UNIT II Basics Elements of VHDL — 7 HOURS

Identifiers – Data objects – Data types – Array – Record – Access types – Incomplete types – File types.

Practical: 3. Encoder and decoder with test bench.
4. Multiplexer and Demultiplexer with test bench — **8 HOURS**

UNIT III Operators and Configurations — 7 HOURS

Operators – Logical – Relational – Shift – Adding – Multiplying – Miscellaneous – Configurations specifications – Configuration declaration – Default rules .

Practical: 5. Memory Module both synchronous and asynchronous – RAM, ROM
6. Design a Clock divider and generation in VLSI Development Kit — **8 HOURS**

UNIT IV Behavioral Modeling — 7 HOURS

Process Statement – Conditional Statement – IF, CASE, LOOP, NEXT and WAIT Statements, Assertion Statement – Exit Statement

Practical: 7. Interfacing of Seven Segment in VLSI Development Kit
8. Interfacing of key board in VLSI Development Kit — **8 HOURS**

UNIT V Structural Modeling and Data Flow Modeling — 7 HOURS

Structural Modeling: Component declaration – Component instantiation – Signals – Variables – Delays
Data Flow Modeling: Concurrent Statement – Concurrent versus Sequential Statement – Conditional Signal Assignment Statement.

Practical: 9. Interfacing of VGA in VLSI Development Kit
10. Interfacing of UART in VLSI Development Kit — **8 HOURS**

TEXT BOOK

A. J. Bhasker, "VHDL Primer", PHI, Fourth Edition, 2015 (Unit I – V).

REFERENCE BOOK

A. Dougles L. Perry, "VHDL", Tata McGraw Hill, Third Edition, 2007

WEB RESOURCES

A. https://www.tutorialspoint.com/vlsi_design/vlsi_design_vhdl_introduction.htm

B. https://www.edutechlearners.com/download/books/A%20VHDL%20Primer%20-%20Jayaram%20Bhasker.pdf

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	L	-	L	-	L	-	S	M	-	-
CO2	S	-	S	-	M	-	S	M	-	-
CO3	L	-	L	-	M	-	S	M	-	-
CO4	S	-	S	-	M	-	S	M	-	-
CO5	S	-	S	-	M	-	S	M	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Theory:

Question Paper Pattern for CIA and Model (50 marks)

CIA and Model Exam (50 Marks is converted into 20 marks)

Section – A (5x4 = 20 Marks)

Either or type

Section – B (5x6 = 30 Marks)

Either or type

CIA Theory (50 Marks)

CIA I – 20 Marks

Model – 20 Marks

Activity – 10 Marks (Lab observation marks converted to 10 Marks)

CE Lab (50 Marks)

Experiment – 45 Marks

Record – 5 Marks

Prepared by
Mr Prasanna Kumar M

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC103	Microwave and Radar Navigation System	Core	45	-	-	3	Theory

PREAMBLE / COURSE OBJECTIVE

This course aims to learn the concepts of Microwave and waveguide. The course helps to understand Microwave amplifiers and oscillators. The course helps the students to understand the principles of Radar navigation system and its applications.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals Knowledge on amplifiers and Oscillators

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / Skill Development

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Classify waveguides and its propagation.	Understand
CO2	Compare the performance of TWT and Klystron	Remember
CO3	Differentiate the types of Microwave Antenna and Arrays	Remember
CO4	Analyze the Performance of Radar and its types	Apply
CO5	Compare the types of CW Radar and FM CW radar	Remember

SYLLABUS

UNIT I Introduction to Microwave [11 Hrs]

Introduction – Maxwell's Equation – Ampere's Law – Faraday's Law – Gauss's law – Wave Equation– TEM/TE/TM/HE Wave Definitions – Wave Guide – Types of Wave Guides – propagation of Wave in the Rectangular Wave Guide – Propagation of TEM Waves – TE and TM Modes – Propagation of TM Waves in Rectangular Wave Guide

UNIT- II Microwave Amplifiers and Oscillators [09 Hrs]

Klystron – Two Cavity Klystron Amplifier - Multi Cavity Klystron – Two Cavity Klystron Oscillator-Reflex Klystron – Traveling Wave Tube(TWT) – Applications – Backward Wave Oscillators – Magnetron: Cavity Magnetron – Sustained Oscillation of Magnetron

UNIT – III Microwave Antennas [09 Hrs]

Quantitative Theory of Short Dipole Antenna – Characteristics Grounded Quarter Wave and Ungrounded Half Wave Antenna – Radiation Resistance and Radiation Pattern – Folded Dipole Antenna and its Applications – Arrays: Broad Side Array and End Fire Array – Loop Antenna – Direction Finding by Adhoc Antenna – Rhombic Antenna – Horn Antenna – Parabolic Antenna

UNIT – IV Principles of Radar System [07 Hrs]

Radar Block Diagram and Operation - Radar Range Equation – Application of Radar System – Minimum Detectable Signal – Receiver Noise – Signal to Noise Ratio – Transmitter Power – Maximum Ambiguous Range

The Radar Receivers – Mixers – Duplexers – Displays

UNIT – V FM Radar and MTI Systems [09 Hrs]

Introduction to Doppler Effect – CW Radar – FM CW Radar – Multiple Frequency CW Radar – Moving Target Indicator(MTI) – Non Coherent MTI – Limitations of MTI Performance

Tracking with Radar – Sequential Lobbing – Conical Scan – Mono Pulse Tracking Radar – Comparison of Trackers

TEXT BOOKS

A. M.Kulkarni, "Microwave and Radar Engineering", Umesh Publications, Fifth Edition, 2014 (Unit I-II)

B. K.D.Prasad, "Antenna and Wave Propagation", Sathya pragasan Publication, Sixth Edition, 2019 (Unit III)

C. Merrill Scholnik, "Radar and Navigation", Tata McGraw Hill Publications, Third Edition, 1992 (Unit IV- V)

REFERENCE BOOK

A. Peter A. Rizzi, " Microwave Engineering Passive circuits", PHI Publication, 2009

WEB RESOURCES

A. https://www.tutorialspoint.com/microwave_engineering/microwave_engineering_directional_couplers.htm
B. https://www.tutorialspoint.com/antenna_theory/antenna_theory_types_of_propagation.htm
C. https://www.tutorialspoint.com/radar_systems/index.htm

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	-	-	S	S	L	-	M	-	-
CO2	S	-	-	M	S	L	-	L	-	-
CO3	M	-	-	S	S	L	-	M	-	-
CO4	M	-	-	M	S	S	-	S	-	-
CO5	M	-	-	M	S	S	-	S	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Prepared by
Mr Ramesh A P

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC104	Digital Communication and Network Techniques	Core	55	-	-	4	Theory

PREAMBLE / COURSE OBJECTIVE

This course aims at understand the basics of Digital Communication in terms of various modulations and the time and frequency domain analysis of the signals. The course helps the students to understand the categories of networks, layer and their function. The course helps the students to Study the various components of LAN network as the operation of network security.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals Knowledge on Basic Digital Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / **Employability** / Skill Development

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Analyze the performance of a digital communication system in terms of various modulations	Understand
CO2	List and describe the categories of Networks.	Remember
CO3	Differentiate the OSI layers and their function	Understand
CO4	Identify the components of LAN implementation	Understand
CO5	Analyze the major issues and technologies in network security	Apply

SYLLABUS

UNIT I Introduction to Digital Communication Systems — 14 HOURS

Communication Links – Data Communication Systems- Synchronous and Asynchronous data – Serial Vs Parallel Communication.

Pulse Modulation: sampling Theory – PAM, PWM, PPM Modulation and detection – TDM – FDM - PCM principles -Data Modulation- ASK- FSK-PSK-DPSK.

UNIT II Structure of Network Communication — 09 HOURS

Network Topologies – Fundamentals of communication theory – Synchronizing Network components- Communication Protocols – Categories of Networks –Internet Works – Transmission Mode.

UNIT III Layer and Their Functions — 14 HOURS

OSI Reference Model – Physical Layer – Data Layer – Network Layer – Transport Session and application layer

MODEM: Modulation Techniques – Multilevel Transmission – Advance in Modem

SWITCHING: Circuit Switching – Message Switching – Compressing.

UNIT IV LAN Network — 9 HOURS

LAN Definition – Major Components of LAN – Protocols – IEEE Standards – CSMA/CD –Token Ring – Token Bus – FDDI – Logical Link Control- Bridge-Router-Repeater-Gateway- HUB.

UNIT V SONET/Network Security — 9 HOURS

Synchronous Transport signals - Physical Configuration - SONET Layers - SONET Frame - Multiplexing STS Frame, VLAN, VPN - Four Aspect of Security:- Privacy - Digital Signature - PGP-Access Authorization.

TEXT BOOK

A. Behrouz A. Forouzan, " Data Communication and Networking", Tata McGraw Hill, Fifth Edition, 2013 (Unit I – V)

REFERENCE BOOKS

A. Prokis J G, "Digital Communication" TMH, Fifth Edition, 2007
B. A S. Tanenbaum, "Computer Networks" PHI, Fifth Edition, 2011
C. Ulysses Black, "Data Communication and Distributed Network", PHI, Sixth Edition, 2008

WEB RESOURCES

A. https://www.gcekbpatna.ac.in/lecture_notes/DCCN_LN_Part1_BY_RPN_GCEK.pdf
B. https://www.tutorialspoint.com/data_communication_computer_network/data_communication_computer_network_tutorial.pdf
C. http://121.241.25.64/myweb_test/syllFybscit/dcn.pdf

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	-	-	S	-	S	-	-	-	-	S
CO2	S	-	L	S	S	-	-	-	-	S
CO3	-	-	S	S	M	-	-	-	-	-
CO4	S	-	M	S	S	-	-	-	-	-
CO5	-	-	L	-	M	S	-	S	S	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Prepared by
Dr Thamarai selvan M

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC105	PRACTICAL –I Embedded System Lab	Core	-	-	50	4	PRACTICAL

PREAMBLE / COURSE OBJECTIVE

This course aims to train students to work on 16 bit microcontroller and low power mode operations The course helps the students to develop high level programming skills and interface communication protocol. The reviews and access I/O devices with MSD430.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals Knowledge on Basic Microprocessor and Microcontrollers

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	To program the 16 bit microcontroller.	Remember
CO2	Establish communication between MSP430 and external devices by using protocol	Apply
CO3	To interface I/O devices with MSP430 hardware.	Remember
CO4	Select and apply low power active and standard nodes.	Apply

SYLLABUS

ANY TEN EXPERIMENTS:

1. Interfacing and programming GPIO ports in C using MSP430 (blinking LEDs , push buttons)
   - Blinking LEDs , push buttons
   - Interfacing 7 Segment Display
   - Interfacing LCD
2. Usage of Low Power Modes:
   - Use MSPEXP430 as hardware platform and demonstrate the low power modes and measure the active mode and standby mode current.
3. Interrupt programming examples through GPIOs
4. PWM generation using Timer on MSP430 GPIO
5. Interfacing potentiometer with MSP430
6. PWM based Speed Control of Motor controlled by potentiometer connected to MSP430 GPIO
7. Using ULP advisor in Code Composer Studio on MSP430
8. Connect the MSP430 to terminal on PC and echo back the data
9. Master Slave Communication between 2 MSP430s using SPI
10. A basic Wi-Fi application – Communication between two MSP430 based sensor nodes
11. Enable Energy Trace and Energy Trace ++ modes in CCS for any of the above [exp. 4-7]
12. Compute Total Energy, and Estimated life time of a battery

WEB RESOURCES

A. http://www.ece.utep.edu/courses/web3376/MSP430_Labs.html

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	M	M	S	S	M	-	S	L	S
CO2	S	M	M	S	S	M	-	S	S	S
CO3	S	M	M	S	S	M	-	S	S	S
CO4	S	M	M	S	S	M	-	S	L	S

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Prepared by
Ms Indira S

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MECE01	Power Electronics and Control Systems	DSE	55	-	-	4	Theory

PREAMBLE / COURSE OBJECTIVE

This course aims to understand the various controls of dc drivers and the students should be able to learn the type of control System, classification of control system, analysis and design.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Basic Knowledge on Basic Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Identify the working of power electronic devices	Remember
CO2	Understand the concept of power drivers	Understand
CO3	Analyze the concepts of open and closed loop control systems.	Apply
CO4	Analyze the stability of closed loop system	Apply
CO5	Apply the control techniques to any electrical systems	Apply

SYLLABUS

UNIT I Power Devices and Gate Commutation Device **10 HOURS**

Need for semiconductor power devices, Power diodes, Enhancement of reverse blocking capacity, Introduction to family of thyristors.

Gate turn off thyristors (GTO) - Power Bipolar Junction transistors (Power BJT) MOSFET- IGBT/IGT and Free Wheeling diode.

UNIT II Driver Circuits **10 HOURS**

Introduction - Gate Drive Circuits for power MOSFET - Gate and device capacitance - Different Driver circuits: CMOS Based driver – Open Collector TTL driver -Bipolar driver - Isolated gate driver - Opto coupler driver

UNIT III Control Systems **12 HOURS**

Introduction to Control Systems: Open Loop and Closed Loop System - Classification of Control System -Transfer Functions - Block Diagram Reduction Rules - Signal Flow Graph - Manson's Gain Formula - Advantages and disadvantages of Open loop System

UNIT IV Time Domain Performance **12 HOURS**

Zero Order, First Order and Second Order System – Unit Step Response and Ramp Response of First Order – Steady State Error for Ramp Response of Second Order – Hurwitz Roughs Stability Criterion – Procedure in Roughs Stability

UNIT V Frequency Domain Analysis **11HOURS**

Correlation between time and frequency response, Polar and inverse polar plots, frequency domain specifications, Logarithmic plots (Bode Plots), gain and phase margins, Nyquist stability criterion, relative stability using Nyquist criterion.

TEXT BOOKS

A. Muhammad Rashid, "Power Electronics Circuits, Devices and Applications", PHI II Edition, Fourth Edition,2017.(Unit I – II)
B. Nagoor Kani, "Control System Engineering" RBA Publications, Third Edition 2017 (Unit III-IV)
C. Katshiko Ogata, "Modern Control Engineering", PHI, Fifth Edition, 2010 (Unit V)

REFERENCE BOOKS

A. P.C. Sen, "Power Electronics", Tata McGraw Hill International, Third Edition 2008
B M.S.Jamil Asghar, "Power Electronics", PHI, Eighth Edition, 2011.

WEB RESOURCES

A. https://www.tutorialspoint.com/power_electronics/index.htm

B. https://www.slideshare.net/hareeshang/unit-1-introduction-to-control-systems

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	S	M	S	S	L	-	-	-	-
CO2	-	S	M	S	S	-	-	M	-	-
CO3	-	-	S	S	S	-	-	M	S	-
CO4	-	-	S	S	S		-	-	S	
CO5	S	S	M	S	S	-	-	M	-	

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Prepared by
Dr Poornima K

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MECE02	Fiber Optic Communication	DSE	55		-	4	Theory

PREAMBLE / COURSE OBJECTIVE

This Course aims to basic elements of optical fiber transmission link, fiber modes configurations and structures. The course helps to understand the different kind of losses, signal distortion, SM fibers and should able to learn the various optical sources, materials and fiber splicing . This course helps to understand the fiber optical receivers and noise performance in photo detector and able to learn link budget, WDM, solutions and SONET/SDH
network.

PREREQUISITE

Under Graduate Level: Fundamental knowledge on Digital ICs and devices.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Demonstrate an understanding of optical fiber communication link, structure, propagation and transmission properties of an optical fiber.	Apply
CO2	Estimate the losses and analyze the propagation characteristics of an optical signal in different types of fibers	Understand
CO3	Describe the principles of optical sources and power launching-coupling methods.	Understand
CO4	Compare the characteristics of fiber optic receivers	Remember
CO5	Design a fiber optic link based on budgets and assess the different techniques to improve the capacity of the system.	Apply

SYLLABUS

UNIT I Introduction to Optical Fiber — 11 HOURS

Evolution of fiber Optic system – Element of an Optical Fiber Transmission link – Ray Optics – Optical Fiber Modes and Configurations – Mode theory of Circular Wave guides – Overview of Modes – Key Modal concepts – Linearly Polarized Modes – Single Mode Fibers – Graded Index fiber structure.

UNIT II Signal Degradation in Optical Fiber — 11 HOURS

Attenuation – Absorption losses, Scattering losses, Bending Losses, Core and Cladding losses, Signal Distortion in Optical Wave guides – Information Capacity determination – Group Delay – Material Dispersion, Wave guide Dispersion, Signal distortion in SM fibers – Polarization Mode dispersion, Intermodal dispersion, Pulse Broadening in GI fibers – Mode Coupling – Design Optimization of SM fibers – RI profile and cut-off wavelength..

UNIT III Fiber Optical Sources — 11 HOURS

Direct and indirect Band gap materials – LED structures – Light source materials – Quantum efficiency and LED power, Modulation of a LED, Laser Diodes – Modes and Threshold condition – Rate equations – External Quantum efficiency – Resonant frequencies – Laser Diodes structures and radiation patterns – Single Mode lasers – Modulation of Laser Diodes, Temperature effects, Introduction to Quantum laser, Fiber amplifiers.

UNIT IV Fiber Optical Receivers — 11 HOURS

PIN and APD diodes – Photo detector noise, SNR, Detector Response time, Avalanche multiplication Noise – Comparison of Photo detectors – Fundamental Receiver Operation – preamplifiers - Error Sources – Receiver Configuration – Probability of Error – The Quantum Limit.

UNIT V Digital Transmission System — 11 HOURS

Point-to-Point links – System considerations – Fiber Splicing and connectors – Link Power budget – Rise-time budget – Noise Effects on System Performance – Operational Principals of WDM, Solutions.

TEXT BOOKS

A. Subir Kumar Sarkar, "Optical Fibres and Optical Communication Systems", S. Chand& Company Ltd, Fifth Edition 2008. [Unit I, II, III& V]

B. Gerd Keiser, —Optical Fiber Communication Tata McGraw– Hill education private Limited,NewDelhi, Fifth Edition,2008,Reprint 2009. (Unit-IV)

REFERENCE BOOKS

A. J.Senior,—Optical Communication, Principles and Practice ‖, Prentice Hall of India, third Edition,2004.

B. J.Gower,—Optical Communication System ‖,Prentice Hall of India,2001

C. Yarvi.A.‖ Quantum Eletronics ‖, John Wiley Fourth edition,1995

WEB RESOURCES

A. https://www.tutorialspoint.com/principles_of_communication/principles_of_optical_fiber_communications.htm

B. https://www.tutorialspoint.com/data_communication_computer_network/digital_transmission.htm

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	P10
CO1	S	-	-	L	-	-	-	-	-	-
CO2	S	M	-	L	M	-	-	-	-	-
CO3	-	-	-	S	S	-	-	M	-	-
CO4	-	M	S	S	M	-	-	M	-	-
CO5	-	S	S	M	M	L	-	-	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

A.P.Ramesh

Prepared by
Mr Ramesh A P

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Approved by
Dr Poornima K

SEMESTER I

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MECE03	Microprocessor and Microcontroller	DSE	55		-	4	Theory

PREAMBLE / COURSE OBJECTIVE

This course helps students to learn about the Hardware of Microprocessor and its interfacing. The course makes the students to know the Microcontroller architecture and to develop programming skill to interface various external devices.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISTE

Under Graduate Level - Fundamental knowledge on Digital ICs and devices.

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Explain the architecture of Microprocessors and Microcontroller	Remember
CO2	Differentiate the operation of Microprocessor and Microcontroller	Understand
CO3	Interface different external peripheral devices with Microprocessors and Microcontroller	Apply
CO4	Analyze a problem and formulate appropriate computing solution for processor or controller based application	Apply
CO5	Develop an assembly language program for specified application	Apply

SYLLABUS

UNIT I 8085 Microprocessors **11 HOURS**

Introduction to Microprocessor 8085 – Architecture- Instruction Set - Data Transfer Instructions – Arithmetic Instructions – logical instructions –Branch Instructions – Stack – I/O and Machine Control Instructions - Addressing Modes- Programming the 8085 Microprocessor – Simple Programs – Delay Program.

UNIT II 8086 Microprocessors **12 HOURS**

Introduction of Microprocessor 8086: Architecture, Addressing modes, instruction set, interrupts Programming, Memory and I/O interfacing. - The 8255A Programming Peripheral Interface – Block Diagram of 8255A, Simple I/O and BSR mode- Block Diagram of 8259 Interrupt Controller – Programming the 8259A –Block diagram of 8253 Timer/ Counter.

UNIT III 8051 Microcontroller **12 HOURS**

Introduction to microcontroller – Microcontroller vs. Microprocessor –Types of Microcontrollers– CISC and RISC Architecture of Microcontrollers – 8051 Microcontroller – Block diagram – I/O pins – 8051ports and circuits- Programming Basics – Introduction to machine instruction and assembly – Instruction cycle –Addressing modes – Data transfer instruction – Data and Bit manipulation Instruction – Arithmetic Instruction.

UNIT IV 8051 Peripherals **10 HOURS**

Timer and Counters: Timer modes of operation-Programming 8051 timers- Counters-Programming counters- Serial Communication-8051 connection to RS232-serial communication programming-Interrupts-Interrupts control and Priority.

UNIT V 8051 Applications **10 HOURS**

Microcontroller Design – Testing the design – Timing and subroutine – Lookup table – Interfacing keyboard – LED/LCD Interface-stepper motor interface – ADC interface – DAC interface.

TEXT BOOKS

A. Ramesh S. Goankar, "Microprocessor Architecture, Programming, and Applications with the 8085", Penram International Publishing, Fifth Edition, 2011.
B. D. V. Hall. Microprocessors and Interfacing, TMGH. 2'1 edition 2006.
C. Kenneth. J. Ayala. The 8051Microcontroller, 3rd edition, Cengage learning, 2010.

REFERENCE BOOKS

A. A. K. Ray and K.M. Bhurchandani, "Advanced Microprocessors and Peripherals" - TMH, 2nd edition 2006.
B. K.Uma Rao, Andhe Pallavi,, "The 8051 Microcontrollers, Architecture and programming and Applications" - Pearson, 2009.
C. By Liu and GA Gibson "Micro Computer System 8086/8088 Family Architecture. Programming and Design" PHI, 2nd Ed.,2006
D. Ajay. V. Deshmukh "Microcontrollers and application", TMGH. 2005.

WEB RESOURCES

A. https://www.tutorialspoint.com/microprocessor/microprocessor_8085_architecture.htm
B. http://examradar.com/8086-microprocessor/
C. https://www.tutorialspoint.com/microprocessor/microcontrollers_8051_architecture.htm

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	P10
CO1	S	-	-	L	-	-	-	-	-	S
CO2	S	-	-	L	M	-	-	-	-	S
CO3	S	-	-	-	S	-	-	M	-	S
CO4	S	-	-	L	M	-	-	M	-	S
CO5	-	-	-	-	M	L	-	S	S	S

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Prepared by
Ms Indira S

Verified by
Dr Thamarai selvan M

Approved by
Dr Poornima K

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC201	Arduino Programming and lab	**Core**	**75**	-	-	**5**	**INTEGRATED (THEORY & PRACTICAL)**

PREAMBLE / COURSE OBJECTIVE

The course helps the students.

- To impart knowledge of the Hardware Architecture and use the development board.
- To develop programs by using AVR Microcontrollers and Arduino IDE
- To configure library and to design & develop I/O specific applications
- To apply various Communication protocols.
- To interface various sensor and motors with Arduino and to construct robot.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals knowledge on Basic Microprocessor and Microcontrollers

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be able to

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Describe the Hardware architecture of the AVR Microcontroller and use development board	Apply
CO2	Develop programs by using AVR Microcontrollers and Arduino IDE.	Apply
CO3	Library and develop I/O applications using Arduino.	Apply
CO4	Implement application by using communication protocol.	Apply
CO5	Interface various sensors and motors for real time applications and construct Robot for small applications.	Apply

SYLLABUS

Unit I: AVR ATmega328p RISC Microcontroller Architecture **7 Hours**

AVR family Architecture- The register file- ALU – Memory Access and instruction execution – EEPROM – Ports – SRAM – Timer – UART – Power down modes.

Practical **8 Hours**

1 Interfacing LED

2 Interfacing Seven Segment Display

Unit II : Introduction And Programming To Arduino **7Hours**

Introduction-Getting started with Arduino IDE- C Language Basics- Functions-Arrays and Strings- Input and Output-Digital and Analog- Variables, Looping statements, Logical Operators, Mathematical operators, Programming with Arduino IDE, Compiling and Debugging using IDE.

Practical **8 Hours**

3 Interfacing matrix Keypad

4 Voltmeter Reading

Unit III: Library And I/O Functions **7Hours**

Standard Arduino Library- Advanced I/O- Interrupts- Data storage – LCD Displays

Practical **8Hours**

5 Interfacing LCD

6 Interfacing IR Obstacle Sensor

Unit IV: Arduino Communication **7Hours**

Network Communication (Wi-Fi) -Arduino Ethernet Programming - Serial Communication: UART Programming – I2C (Inter Integrated Circuit)-SPI(Serial Peripheral Interface).

Practical **8 Hours**

7 Interfacing Temperature sensor

8 Interfacing Ultrasonic Sensor

UNIT – V: Applications – Interfacing with Sensors and Motors **7Hours**

Humidity Sensor-Temperature Sensor-Water Detector Sensor-PIR Sensor – Ultrasonic Sensor – DC Motor – Stepper Motor-Servo Motor.

Practical **8 Hours**

9 Interfacing Humidity Sensor

10 Interfacing DC / Stepper / Servo motor

TEXT BOOKS

A. Dhananjay Gadre, Programming and Customizing the AVR Microcontroller, Tata McGraw Hill, 2012. (Unit - I)

B. Massimo Banzi, "Getting Started with Arduino: The Open Source", Shroff Publishers & Distributors Pvt., Ltd., 2014. (Unit II -III)

C. Simon Monk, "Programming Arduino: Getting Started with Sketches", McGraw-Hill Education, Second Edition,2016. (Unit II -III)

D. www.tutorialspoint.com/arduino (Unit IV-V)

REFERENCE BOOK

A. Muhammad Ali Mazidi, Darmad Naimi and Sepehr Naimi, "The AVR Microcontroller and Embedded Systems using Assembly and C", Pearson First Edition, 2015.

WEB RESOURCES

A. www.arduino.cc

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	S	-	M	L	-	-	M	-	-
CO2	S	L	-	S	L	-	-	M	-	-
CO3	S	S	-	M	L	-	-	M	-	-
CO4	S	L	-	S	S	-	-	M	-	-
CO5	S	L	-	S	S	-	-	M	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Question Paper Pattern for CIA I & Model Exam

(50 Marks converted to 20 Marks)

SECTION – A (5 x 4 = 20 Marks)
Descriptive Questions (Either or type)
SECTION – B (5 x 6 = 30 Marks)
Descriptive Questions (Either or type)

CIA Theory (50 Marks)

- **CIA I for 20 Marks**
- **Model for 20 Marks**
- **Activity for 10 Marks (Lab observation marks converted to 10 Marks)**

CE Lab (50 Marks)

- **Experiment for 45 Marks**
- **Record for 5 Marks**

Mr Sathish Kumar V
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC202	VERILOG Programming	Core	55	-	-	4	THEORY

PREAMBLE / COURSE OBJECTIVE

- To emphasis on writing synthesizable code and simulation codes.
- To make the student to write a Verilog HDL codes using Structural, Dataflow and behavioral coding styles.
- To impart the knowledge on user defined primitives and on their applications.
- To understand the verification concept in Verilog HDL

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals knowledge on basic Digital Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / Skill Development

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Apply the design flow concept of in creating the hardware models	Remember
CO2	Apply different modeling concepts in design a digital hardware models.	Understand
CO3	Create behavioral style of modeling codes by using conditional, looping and timing functions.	Apply
CO4	Model and synthesize the codes using delay concept for a real time applications.	Apply
CO5	Solve architectural problems by proper partitioning and verifying it using formal verification.	Apply

SYLLABUS

UNIT - I Digital Design With Verilog HDL **11 Hours**

Evolution of CAD - Emergence of HDLs, Typical HDL based design flow, Trends in HDLs - Hierarchical Modeling Concepts - Design methodology - modules and instances - components of a simulation - design block - stimulus block. Basic Concepts of Lexical conventions - data types - system tasks, compiler directives.

UNIT - II Gate Level Modeling & Data Flow Modeling **11 Hours**

Modules and Ports- Module definition - port declaration and connecting ports - hierarchical name.

Gate Level Modeling: Gate Types – Gate Delays with Examples.

Dataflow Modeling: Continuous Assignments – Delays – Expressions, Operators and Operands – Operator Types.

UNIT - III Behavioral Modeling **11 Hours**

Behavioral Modeling: Structured procedures - procedural assignments - Timing Controls - Conditional statements - Multiway branching – Loops - sequential and parallel blocks – Tasks and Functions - Differences between tasks and functions.

UNIT - IV Advanced Verilog Topics Timing And Delays **11 Hours**

Types of delay models – path delay modeling – Timing Checks – Delay back annotation – Switch level modeling Elements – MOS switches and CMOS switches – Bidirectional switches - UDP basics – Combinational UDP Definition – Sequential UDP – Guidelines for UDP Design.

UNIT - V Advanced Verification Techniques **11 Hours**

Verification of the gate level net list –Verilog coding style - Design partitioning – Horizontal partitioning – Vertical partitioning – Parallelizing design structure - Advanced verification techniques: Traditional verification flow – Architectural Modeling – Functional Verification Environment - Assertion checking -Formal verification.

TEXT BOOK

A. Samir Palnitkar "Verilog HDL" Second Edition IEEE 1364-2012 Compliant (Unit I - V)

REFERENCE BOOK

A. J.Bhasker, "Verilog HDL Synthesis, A Practical Primer", BS Publication, 3rd Edition, 2009

B. Micheal D. Ciletti, "Advanced Digital Design with the Verilog HDL", PHI publications, Indian reprint, 2011

WEB RESOURCES

A. https://www.tutorialspoint.com/vlsi_design/vlsi_design_verilog_introduction.htm

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	M	-	-	-	-	-	S	-	-	-
CO2	M	-	-	S	-	-	S	-	-	-
CO3	M	-	-	S	-	-	S	-	-	-
CO4	M	-	-	S	-	-	S	-	-	-
CO5	M	-	-	-	-	-	S	-	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Mr Prasanna Kumar M
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC203	PRACTICAL –II VERILOG Programming lab	**Core**	-	-	**48**	**4**	**PRACTICAL**

PREAMBLE / COURSE OBJECTIVE

This course aims

- To enable the students to understand the various programming styles of Verilog design.
- To understand about RTL code in various hardware components interface in a FPGA chip.
- To understand the software and hardware needs of Verilog.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals Knowledge on amplifiers and Oscillators

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / Skill Development

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Write codes in Verilog HDL for synthesis and simulation of digital circuits.	Understand
CO2	Design a module for real time applications.	Apply
CO3	Write Verilog test benches codes for testing the circuit.	Apply
CO4	Interface modules with FPGA by writing appropriate codes.	Apply

SYLLABUS

ANY TEN EXPERIMENTS:

1. Verification of logic gates with test bench.
2. Four bit full adder and Subtractor in single module wit test bench.
3. Encoder and decoder with test bench.
4. Multiplexer and Demultiplexer with test bench.
5. Memory Module RAM and ROM.
6. Design a Finite State Machine and check the result with help of test bench.
7. Design a Clock divider and generation in VLSI Development Kit.
8. Design a Counter and display it in the Seven Segment of VLSI Development Kit.
9. Interfacing of key board in VLSI Development Kit.
10. Interfacing of VGA in VLSI Development Kit.
11. Interfacing of Audio Codec in VLSI Development Kit.
12. Design an UART module.
13. Interfacing of Liquid Crystal Display.
14. Interfacing of GLCD.
15. Interfacing of Camera Module.

WEB RESOURCES

- https://www.tutorialspoint.com/vlsi_design/vlsi_design_verilog_introduction.htm

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	-	-	-	-	S	-	S	-	-	M
CO2	-	-	-	M	S	-	S	-	-	M
CO3	-	-	-	M	S	-	S	-	-	M
CO4	-	-	-	M	S	-	S	-	-	M
CO5	-	-	-	-	S	-	S	-	-	M

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Mr Prasanna kumar M
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC204	Analysis and Processing of Signals	**Core**	**55**	-	-	**4**	**Theory**

PREAMBLE / COURSE OBJECTIVE

This course aims

- To study the concepts and properties associated with the signals and systems.
- To familiarize with the techniques suitable for analyzing and synthesizing both continuous and discrete time systems.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals Knowledge on Basic Digital Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / **Employability** / Skill Development

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Compare various types of signals and systems.	Remember
CO2	Compute and interpret convolution and correlation systems for random process.	Remember
CO3	Use Fourier transform to analyze continuous time signals and systems.	Understand
CO4	Use discrete time Fourier transform to analyze discrete time signals and systems. Structure for realization of IIR and FIR filters.	Understand
CO5	Demonstrate the production of speech, voice recognition and Image capturing.	Apply

SYLLABUS

UNIT I Signals and Systems **11 Hours**

Signals: classification of signals: Continuous time signals- discrete time signals- singularity function Systems: Classification of systems: Continuous time systems- Discrete time systems- Representation of systems.

UNIT - II Convolution and Correlation **11Hours**

Discrete convolution- Properties of Convolution-Linear convolution- Circular convolution- Graphical method- Linear convolution Vs Circular Convolution.

Correlation: Cross correlation – Auto Correlation.

UNIT-III DFT **11 Hours**

DFT – Properties of the DFT– Notation and formula of the real DFT – DFT basic functions – Synthesis and analysis of DFT –Synthesis and calculating the inverse DFT- Applications of the DFT.

UNIT – IV FFT & Filters **11 Hours**

FFT- Radix 2FFT-Working Principle of FFT – Speed and precision comparison - FIR Filter: Introduction- Design techniques: Fourier series method- Frequency sampling method IIR Filter: Introduction-Design techniques- Impulse invariant method – Bilinear transformation method.

UNIT – V Applications **11 Hours**

Audio processing – Human hearing – Timbre – Sound quality Vs Data rate – High fidelity audio – Compounding – Speech synthesis and Recognition – Image formulation and Display: Digital image structure– Cameras and End Eyes – Television video signals – Other image acquisition and display – Brightness and contrast adjustments – Warping.

A..S. Salivahanan, A. Vallavaraj, C. Gnanapriya "Digital Signal Processing", TMH, 2th Edition, 2010 (Unit I– IV)

B. Steven. W. Smith, "The Scientist and Engineers guide to DSP", California Technical Publishing California, 1999 (Unit V)

REFERENCE BOOKS

A. John. G. Proakis and Dimities G. Manolaks, "Digital Signal Processing", PHI Publications, 2003

WEB RESOURCES

A. https://ocw.mit.edu/resources/res-6-008-digital-signal-processing-spring-2011

B. https://terpconnect.umd.edu/~toh/spectrum/

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	-	-	-	-	S	-	-	-	S	-
CO2	S	-	L	-	S	-	-	-	S	-
CO3	-	-	-	-	S	M	-	-	S	-
CO4	-	-	-	-	S	S	-	-	S	-
CO5	-	-	-	-	S	S	-	-	S	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Ms Indira S
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayashcela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC205	Automotive Embedded Systems	**Core**	**44**	-	-	**3**	**THEORY**

PREAMBLE / COURSE OBJECTIVE

This course aims

- To enable the students to understand the various architecture and technologies used in automotive vehicles.
- It also helps them to learn the embedded communications used in Automotive.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals Knowledge on Basic Microprocessor and Microcontrollers

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Design and develop automotive embedded systems.	Apply
CO2	Analyze various embedded products used in automotive industry.	Remember
CO3	Evaluate the opportunities involving technology, a product or a service required for developing a startup idea used for automotive applications	Apply
CO4	Interface devices and build a complete system.	Apply

SYLLABUS

UNIT-I: Automotive Architecture **8Hours**

General Context - Functional domains - Standardized components, Models and Processes – Certification issue of safety critical in Vehicle embedded systems – ESD.

UNIT-II: Intelligent Vehicle Technologies **8Hours**

Road transport and its evolution – New technologies LiDAR remote sensing – Dependability Issues – Autonomous Car - Wireless car

UNIT-III: Automotive Protocols **8Hours**

Automotive communication Systems - Characteristics and constraints – In Car Embedded Networks – Middleware Layer – Open issues for Automotive Communication Systems.

UNIT-IV: Embedded Communications **10Hours**

FLEXRAY

Introduction - Event driven verses Time driven communication-Objectives of flex ray-Flex ray communication-Frame format -Communication cycle-Static segment-Dynamic segment.

FLEXCAN

Main requirements of Automotive Networking - Network technologies - CAN features and limitations-Control system - Flex CAN architecture-Flex CAN address CAN limitations-Flex CAN applications.

UNIT – V Embedded Software **10Hours**

Product Lines in Automotive Electronics- Characteristics of Automotive Product Lines – Basic Technology – Global Coordination of Automotive Product line variability – Artifact level variability.

TEXT BOOK

A. NICOLAS NAVET, FRANCAISE SIMONOT –LION, "Automotive Embedded Systems Hand Book" , CRC Press 2009 (Unit I – V)

WEB RESOURCES

A. https://d1.amobbs.com/bbs_upload782111/files_38/ourdev_629261ASTZIF.pdf

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	-	-	M	-	-	-	-	S	-	-
CO2	-	-	M	-	-	S	-	M	-	-
CO3	-	-	M	-	-	M	-	S	-	-
CO4	-	-	S	-	-	-	-	M	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Dr Thamaral selvan M
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MECE04	CRYPTOGRAPHY	**DSE**	**55**	-	-	**4**	**Theory**

PREAMBLE / COURSE OBJECTIVE

- To understand the basic concept of cryptography and network security their function.
- To be familiar with cryptographic techniques for secure communication of two parties over an insecure channel.
- To illustrate how network security and management mechanisms employ cryptography to prevent, detect, and mitigate security threats against the network

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Basic Knowledge on Basic Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Account for the cryptographic theories, principles and techniques that are used to establish security properties.	Understand
CO2	Analyze and use methods for cryptography.	Remember
CO3	Reflect about limits and applicability of methods for network security.	Apply
CO4	Acquired the concept cryptanalysis in wireless techniques.	Understand
CO5	Analyze the principle of Cipher technology in IP security.	Apply

SYLLABUS

UNIT - I Introduction **10 Hours**

Computer security concepts – The OSI Security Architecture - Security attacks- Security Services - – Security Mechanisms – A Model for Network security

UNIT - II Cryptography **13 Hours**

Symmetric Encryption Principles – Symmetric Block Encryption Algorithms – Random and Pseudorandom Numbers – Stream Ciphers and RC4 – Cipher Block modes of operation. Approaches to message authentication – Secure Hash Functions – Message authentication codes – Public key cryptography Principles - Public key cryptography Algorithms - Digital Signature.

UNIT - III Network Security **11 Hours**

Symmetric key Distribution using symmetric encryption – Kerberos – key distribution using asymmetric encryption – x.509 certificates – Public key infrastructure – Federated identity management.

UNIT - IV Wireless Network Security **11 Hours**

IEEE 802.11 wireless LAN overview – IEEE 802.11 I wireless LAN Security – Wireless Application Protocol overview – wireless transport layer security - WAP End to End Security.

UNIT – V IP Security **10 Hours**

IP Security – IP Security policy – Encapsulating security associations – Internet key exchange – Cryptographic suites.

TEXT BOOK

A. Willaim Stallings, "Network Security Essentials", PHI, 4th Edition, 2011 (Unit I – V)

REFERENCE BOOKS

A. Douglas Stinson, "Cryptography Theory and Practice", 2nd Edition, Chapman & Hall/CRC.
B. A. Forouzan, "Cryptography & Network Security", Tata Mc Graw Hil

WEB RESOURCES

A. http://index-of.es/Hack/Network%20Security%20Essentials%204th%20Edition.pdf

B. http://www.uoitc.edu.iq/images/documents/informatics-institute/Competitive_exam/Cryptography_and_Network_Security.pdf

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	S	M	-	-	-	-	L	-	-
CO2	-	-	M	-	S	-	-	L	-	-
CO3	S	-	M	-	-	-	-	L	-	-
CO4	-	-	M	S	-	-	-	L	-	-
CO5	-	-	M	S	-	-	-	L	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Mr Ashok Kumar K
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MECE05	Digital CMOS VLSI Design	DSE	55	-	-	4	Theory

PREAMBLE / COURSE OBJECTIVE

This course aims

- To explain the operation of different MOS transistors and their characteristics like I-V and C-V characteristics.
- To discuss basic CMOS logic gates, implementation of multiplexers using tristate gates.
- To analyze different delays and power dissipation in number of stages.
- To understand the design of combinational circuits using ratioed, cascade and dynamic logic.
- To design different types of sequential circuits.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level –Basic Knowledge on Basic Electronics

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	understand the fundamental areas of applications for the Integrated Circuits	Understand
CO2	Identify the basic design structures using CMOS logic	Remember
CO3	Design the different delays like RC, Linear etc and to know how to calculate static and dynamic power	Apply
CO4	Analyze to draw different ratioed logic circuits and cascade circuits	Remember

SYLLABUS

Unit I MOS Transistor Theory: **11 Hours**

A Brief History, MOS Transistors, Long-Channel I-V Characteristics, C-V Characteristics, Non ideal I-V, Device Models.

Unit II Logic gates: **11 Hours**

CMOS Logic Gates (The Inverter, NAND and NOR Gate, Compound Gates), Pass Transistors and Transmission Gates Tristate, Tristate, Multiplexers, Sequential Circuits.

Unit III Delay& Power calculations: **11 Hours**

RC Delay Model, Linear Delay Model, Delay in Multistage Logic Networks, Choosing the Best Number of Stages, Dynamic Power, Static Power.

Unit IV Design of combinational circuits: **10 Hours**

Static CMOS, Rationed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass-Transistor Circuits

Unit V Design of sequential circuits: **12 Hours**

Conventional CMOS Latches &Flip-Flops, Pulsed Latches, Resettable Latches and Flip-Flops, Enabled Latches and Flip-Flops, Incorporating Logic into Latches, Differential Flip-Flops, Dual EdgeTriggered Flip-Flops True Single-Phase-Clock (TSPC) Latches and Flip-Flops.

TEXT BOOKS

A. Weste, N. H. E., Harris, D. M "CMOS VLSI design: a circuits and systems perspective. Boston, Pearson/Addison-Wesley Fourth Edition.2011 (UNIT I –V)

REFERENCE BOOKS

A. S. M. Kang, Y. Leblebici, CMOS Digital Integrated Circuits, 3/e, McGraw Hill, 2012.
B. Jackson, Hodges, Analysis and Design of Digital Integrated circuits, 3/e, McGraw Hill, 2012.
C. Ken Martin, Digital Integrated Circuit Design, Oxford Publications, 2011-

WEB RESOURCES

A. http://swarm.cs.pub.ro/~mbarbulescu/SMPA/CMOS-VLSI-design.pdf
B. http://www.smohanty.org/Teaching/2008Fall_VLSI/MohantyVLSI5Microwind.pdf

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	-	-	M	M	S	-	S	-	-	-
CO2	-	-	L	M	S	-	S	-	-	-
CO3	-	-	L	M	S	-	S	-	-	-
CO4	-	-	M	M	S	-	S	-	-	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Dr Thamarai selvan M
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MECE06	ASIC Design	**DSE-II**	**55**	-	-	**4**	**Theory**

PREAMBLE / COURSE OBJECTIVE

This course aims at understand the basics of ASIC Design. To enable the students to learn about various types of ASIC, concepts and design flow of ASIC and to implement it with Micro wind software.

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISITE

Under Graduate Level – Fundamentals knowledge on VLSI Deign

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / Employability / **Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Describe various ASIC architectures	Understand
CO2	Apply the concept in programming the Logic Cells	Understand
CO3	Apply programming concept in the lower level models	Remember
CO4	Analyze the floor planning for the customized designs	Apply
CO5	Place and Route the signals according to their design flow	Apply

SYLLABUS

UNIT I Introduction to ASIC **11 HOURS**

ASIC Design – Introduction- ASIC Examples- Advantages – Types- Full custom ASIC, Semi – Custom ASIC – Standard cell – Based ASIC – GATE Array – based ASIC, -Channels gate array- Structured gate array – Field –Programmable Gate array- Programmable logic devices structure –PALs –PLDs – Programming of PALs – Field Programmable Gate array – ASIC design flow.

UNIT II Programmable ASIC, Logic cells and I/O cells **11 HOURS**

Anti fuse- Static RAM- EPROM and EEPROM technology, PREP benchmarks - Actel ACT- Shannon's Expansion theorem - ACT2 and ACT3 logic module – Xillinx LCA – Altera FLEX – DC output – AC output - DC input - AC input - clock input- Power input – Xilinx I/O Block – Other I/O cells.

Case Study: Programming of RAM,ROM and other I/O cells.

UNIT III Programmable ASIC Interconnect, software and low level design entry 11 HOURS

Actel ACT – Xillinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 –Altera MAX 9000 – Altera FLEX – Design systems – logic Synthesis – half gate ASIC - Schematic entry – Low level design language – PLA Tools – EDIF – CFI Design representation.

Case Study: Programming the interconnects of various logical level design of families like Altera 5000,7000 and 9000.

UNIT IV ASIC Construction, Floor Planning **11 HOURS**

Physical Design- CAD tools - System partitioning – Estimating ASIC size –Power Dissipation – FPGA partitioning – Partitioning methods – Ratio cut algorithms – Look ahead algorithms - floor planning – Floor planning tools – I/O power Planning – Clock planning.

Case Study: how Partitioning and floor planning will optimize the entire system.

UNIT V Placement and Routing **11 HOURS**

Placement –Measurement of placement – Placement algorithms – Simulated annealing – Timing driven Placement methods - physical design flow –Routing - global routing – detailed routing – special routing

TEXT BOOKS

A. M.J.S. Smith," Application – Specific integrated circuit" – Addison – Wesley Longman Inc, 2 reprint edition, 2000 (Unit I – V)

REFERENCE BOOK

A. Andrew Brown, "VLSI circuits and systems in silicon", Tata Mc Graw Hill Publications, 1991

B. S.D Brown, R.J.Francis, J.Rox , Z.G.Uransesic, " Field Programmable gate arrays" Khuever academic publisher, 1992.

C. S.Y.Kung, H.J.Whilo House, T.Kailath, "VLSI and Modern Signal Processing" PHI Publications, 1985.

WEB RESOURCES

A. https://www.tce.edu/sites/default/files/PDF/14EC770-ASIC-DESIGN-K.Kalyani.pdf

B. http://www.csitsun.pub.ro/resources/asic/CH01.pdf

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	P10
CO1	S	-	-	S	S	-	-	L	-	S
CO2	S	-	-	S	M	-	-	S	-	S
CO3	M	-	-	L	S	-	-	S	-	S
CO4	S	-	-	S	S	S	-	S	-	S
CO5	S	-	-	S	S	S	-	S	-	S

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

Follows common pattern of Internal and External assessment, suggested in the Regulations.

Mr Prasanna kumar M
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT
20MEA01	MACE-I	AEC	40	-	-	2	Theory

PREAMBLE / COURSE OBJECTIVE

This course aims at enhancing the students English language ability, help them write better and communicate effectively, improve their body language, adopt good manners and maintain professional etiquette.

DEPARTMENT OFFERING

TIP Center

PREREQUISTE

UG Completion

EXPECTED SKILL

Communication skills / Soft Skills/ Writing Skills

COURSE OUTCOMES

On successful completion of the course, students will be able to-

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Assess individual skills and set goals	Remember
CO2	Enhance basic English vocabulary	Understand
CO3	Enhance verbal ability using grammar	Apply
CO4	Display good body language, manners and etiquettes at workplace	Apply
CO5	Demonstrate professionalism in speaking and writing at workplace	Apply

SYLLABUS

UNIT I **7 HOURS**

Assessment of individual levels of communication skills, aptitude and employability skills; Psychometric test, SWOT analysis; Planning on setting goals. Introduction to Career planning; Goal setting – Introduction to Soft Skills - Presentation skills - Intra-personal skills

UNIT II **6 HOURS**

Enhancement of Basic English vocabulary; Nouns, Verbs, Tenses, Phrases, Synonyms, Antonyms, and Homonyms Descriptive words - Combining sentences

UNIT III **9 HOURS**

English language enhancement- Business Idioms- Indianisms in English- Common Errors in Pronunciation - Signposts in English- Verbal ability-Articles-Parts of speech-Phrases, clauses and modifiers - errors in tenses – prepositional errors – parallelism errors – mood, conditionals and multiple usages.

UNIT IV **9 HOURS**

English listening- hearing Vs. listening - Nonverbal communication – Appearance, dressing and grooming - Tips to maintain good impression at work - business etiquette – basic postures and gestures and table manners, Body language - dealing with people communication - media etiquette - telephone etiquette, email etiquette

UNIT V **9 HOURS**

Basics of Writing Skills – Sentence Construction – Email Writing. Presentation Skills (Writing) – Effective organization of content – Importance of Presentation in both Writing and Speaking. Communication Process and Barriers – Elimination of stage fear – Impromptu speaking

TEXT BOOKS

A. Service provider adapted text books and study materials

REFERENCE BOOKS

A. Practical English Usage – Michael Swan (Oxford University Press).
B. Learner English – Michael Swan(Cambridge University Press
C. Effective Writing and Speaking – John Seely (Oxford University Press)

WEB RESOURCES

A. www.tefl.net

B. www.busyteacher.org

C. www.englishclub.com

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9
CO1									
CO2									
CO3									
CO4									
CO5									

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN (if deviation from common pattern)

- Total: 100 Marks
- Online exam: 50 Marks
- Oral Evaluation: 50 Marks
- Passing Minimum: 60 %
- External Assessment

Prepared & Verified by
Dr M Thamarai selvan

Approved by
Academic Council

SEMESTER II

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT	ASSESSMENT CODE
20MEC206	**(Summer Project-1 /Internship/Teaching Assignment)**	**SUMMER COURSE-1**	-	-	-	**1**	-

PREAMBLE / COURSE OBJECTIVE

- To understand and gain the knowledge of engineering practices so has to participate and produce engineering project in future
- To Create research and development knowledge for Post graduate students using different types of application software related into electronics field

DEPARTMENT OFFERING

M.Sc Electronics and Communication System

PREREQUISTE

Under Graduate Level – Project / Internship

EXPECTED SKILL

Domain Knowledge / Entrepreneurship / **Employability / Skill Development**

COURSE OUTCOMES

On successful completion of the course, students will be

S. NO.	COURSE OUTCOME	BLOOMS LEVEL
CO1	Apply learned methodologies and techniques to solve the problems.	APPLY
CO2	Design and develop hardware circuits to developed projects	APPLY
CO3	Develop their skills and utilizing internship	APPLY

SYLLABUS

OVERVIEW

"Each student has expected to undergo summer project / internship training work for the period of 15 days at the end of the second semester and required to submit a report in the prescribed format and marks will be awarded accordingly. The student performance will be monitored by the Head of the Department / Class tutor."

TASK

The student can do project in industry or in our lab/ internship in industry.

CONTENT OF THE PROJECT / INTERNSHIP REPORT

PROJECT REPORT

A. Introduction
B. Existing and Proposed System
C. Block Diagram and Explanation
D. Circuit Diagram and Explanation
E. Screen shots Results
F. Conclusion

INTERNSHIP REPORT

A. Introduction
B. Profile of the Company
C. Organization Structure
D. Functioning of Various Departments
E. Key Results of the Study
F. Completed certificate.

MAPPING WITH PROGRAM OUTCOMES

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	P10
CO1	L	-	-	S	S	-	M	S	M	-
CO2	L	-	-	S	S	-	M	S	M	-
C03	L	-	-	S	S	-	M	S	M	-

S- Strong; M-Medium; L-Low

ASSESSMENT PATTERN

Internal Only	
Attendance Regularity	40 Marks
Report Preparation	60 Marks
Total	100 Marks

Dr Thamarai selvan M
(Course Coordinator)

Dr Poornima K
(BoS Chairperson)

Dr Jayasheela D
(Academic Council- Member Secretary)