DEPARTMENT OF ELECTRONICS

S.N.R. SONS COLLEGE

(Autonomous)
(Affiliated to Bharathiar University)
[Re- Accredited with 'A' Grade by NAAC]
[An ISO 9001:2008 Certified Institution]
Coimbatore – 641 006.

M.Sc ELECTRONICS AND COMMUNICATION SYSTEM

SYLLABUS

EFFECTIVE FROM 2015-16

S.N.R.SONS COLLEGE (AUTONOMOUS)
DEPARTMENT OF ELECTRONICS
M.Sc., ELECTRONICS AND COMMUNICATION SYSTEM
(ACADEMIC YEAR 2015 – 2016 ONWARDS)
SCHEME OF EXAMINATION

SEMESTER I:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	15MEC101	8051 Microcontroller and its Applications	5	3	25	75	100
2	15MEC102	Power Electronics and Control Systems	4	3	25	75	100
3	15MEC103	Microwave and RADAR Navigation System	4	3	25	75	100
4	15MEC104	Digital Communication And Network Techniques	4	3	25	75	100
5	15MEC105	**Practical I:** 8051 Microcontroller and its Applications	3	4	40	60	100
6	15MEC106	**Practical II:** Advanced Electronics	3	4	40	60	100
		TOTAL	**23**				**600**

SEMESTER II:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	15MEC201	Embedded System & RTOS Design	4	3	25	75	100
2	15MEC202	VHDL Programming	5	3	25	75	100
3		**Supportive Course – I**	4	3	25	75	100
4	15MEC203 / 15MEC203A / 15MEC203B	**Elective – I**	4	3	25	75	100
5	15MEC204	**Practical III:** Embedded System & RTOS Lab	3	4	40	60	100
6	15MEC205	**Practical IV:** VHDL Programming	3	4	40	60	100
		TOTAL	**23**				**600**

SEMESTER III:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	15MEC301	Analog Device BlackFin DSP	5	3	25	75	100
2	15MEC302	Digital System Design using Verilog	5	3	25	75	100
3		**Supportive Course – II**	4	3	25	75	100
4	15MEC303 / 15MEC303A / 15MEL303B	**Elective – II**	4	3	25	75	100
5	15MEC304	**Practical V**: Analog Device BlackFin DSP	3	4	40	60	100
6	15MEC305	**Practical VI**: Verilog HDL Programming	3	4	40	60	100
7		**IDC** – Inter Department Course Subject to be offered by Other Department	3*	3	-	100	100*
		TOTAL	**24**				**600**

SEMESTER IV:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	15MEC401	MEMS and NEMS	4	3	25	75	100
2	15MEC402	Automotive Embedded Systems	4	3	25	75	100

S.No	Course Code	Course	Credit	Project Report	Viva Voce	Total
3	15MEC403	Project Work and Viva – voce	12	160	40	200
		TOTAL	**20**			**400**

CIA – CONTINUOUS INTERNAL ASSESSMENT

CE – COMPREHENSIVE EXAMINATION

SUPPORTIVE COURSE

S.No	Supportive Course – I	Supportive Course – II
1	Analysis and Processing of signals	Mobile Communication Systems & Standards
2	Robotics and Automation	Digital Image Processing
3	Neural Network and Its Applications	Multimedia Compression Techniques

IDC – Inter Department Course Subject to be offered by Other Department
Fundamentals of Embedded Systems

ELECTIVE:

S.No	Course Code	Elective – I	Course Code	Elective – II
1	15MEC203	Fiber optic Communication	15MEC303	ARM 9 Embedded Processor & Raspberry Pi
2	15MEC203A	High performance communication networks	15MEC303A	Analysis and design of analog IC's
3	15MEC203B	Advanced speech processing	15MEC303B	Advanced Network Techniques

Total Marks: 2200

Total Credits: 90

Dr. G. SENTHIL KUMAR
Chairman, Board of studies in Electronics
S.N.R. Sons College, Coimbatore

SEMESTER – I
8051 MICROCONTROLER AND ITS APPLICATIONS
COURSE CODE: 15MEC101

Instructional hours per week: 5

Objective: To enhance the students to understand the working principles of microcontroller and to get wide knowledge in the field of 8051 microcontroller and its applications.

Unit I: Microprocessor and Microcontroller [11 Hrs]

Introduction – Microprocessor and Microcontrollers – A Microcontroller Survey – The 8051 Architecture – 8051 Microcontroller Hardware

Instruction Set:Addressing Modes – Data Transfer Instruction – Logical Instruction– Arithmetic Instructions – Jump and Call Instructions

Unit II: Microcontroller Design [12 Hrs]

Microcontroller Design: External Memory and Memory Spacing Decoding – Reset and Clock Circuits – Expanding I/O – Memory Mapped I/O – Memory Access Time

Testing the Design: Crystal Test – ROM Test and RAM Test – Time delay generation and calculation – Lookup Tables For The 8051

Unit III: Timer/Counter, Serial Communication and Interrupt Programming [13 Hrs]

Timer / Counter Programming in the 8051: Programming 8051 Timers - Counter Programming Serial Communication: Basic Serial Communication – 8051 Connection to RS232 – 8051 Serial Communication Programming

Interrupt Programming: ss8051 Interrupts – Programming Timer Interrupts – Programming Hardware External Interrupts – Programming the Serial Communication Interrupt Priority in The 8051

Unit IV: Development Tools for Microcontroller Applications [10Hrs]

Development phases of a Microcontroller Based system – Software Development cycle and Applications – Software Development Tools: Integrated Development Environment(IDE) –

Example of an IDE - μ Vision and Tools from KEIL: BL51 Linker/Locator

Emulator and in-Circuit Emulator (ICE): In-circuit Emulator (ICE) – Joint Test Action Group (JTAG) – Logic Analyzer Circuit

Unit V: Interfacing & Application case studies [9 Hrs]

Interfacing an LCD - ADC interface, Interfacing Temperature Sensor – Interfacing a Stepper Motor - Interfacing to the Keyboard - Interfacing a DAC

TEXT BOOKS:

1. Kenneth J. Ayala, "The 8051 Microcontroller Architecture, Programming and Application", Penram International Publications, Second Edition (Unit I – III)

2. Raj Kamal, " MICROCONTROLLERS Architecture, Programming, Interfacing and System Design", Pearson Education, Second Edition (Unit – IV)

3. Muhammad Ali Mazidi, Janice GfillispieMazidi, "The 8051 Microcontroller and Embedded Systems", Pearson Education, LPE 8th reprint 2004 (Unit V)

SEMESTER – I
POWER ELECTRONICS AND CONTROL SYSTEMS
COURSE CODE: 15MEC102

Instructional hours per week: 5

Objective: To enable the students to understand the basic concepts of power controlled circuits and to learn various parameter in control system engineering

Unit I: Power Semiconductors and Gate Commutation Device [12 Hrs]

Thyristor Communication Techniques: Introduction – Natural Commutation – Forced Commutation – Self Commutation – Impulse Commutation – Resonance Pulse Commutation – External Pulse Commutation – Load Side and Line Side Commutation – Complementary Commutation

Gate Commutation Devices: Gate turn off thyristors (GTO) – Power Bipolar Junction transistors (Power BJT) – MOSFET- IGBT/IGT and Free Wheeling diode.

Unit II: Driver Circuits and DC Choppers [10 Hrs]

Introduction – Gate Drive Circuits for power MOSFET – Gate and device capacitance – Different Driver circuits: CMOS Based driver – Open Collector TTL driver – Bipolar driver – Isolated gate driver – Opto coupler driver

DC Choppers: Introduction – Step Down with RL Load – Principle of Step Up Operation

Switch Mode Regulators: Buck Regulators – Boost Regulators – Buck/Boost Regulators – CUK Regulators

Unit III: Invertors and switches [11 Hrs]

Invertors: Introduction – Principle of Operations – Single Phase Bridge Invertors – Three Phase Invertors

AC Voltage Controller: Introduction – Principles of ON/OFF Control and Phase Control

Static Switches: Introduction – Single Phase and Three Phases AC Switches – DC Switches – Solid State Relays

Unit IV: Control System and Feedback Characteristics [11 Hrs]

Open Loop and Closed Loop System – Classification of Control System – Transfer Functions - Block Diagram Reduction Rules – Signal Flow Graph – Manson's Gain Formula – Advantages and disadvantages of Open loop System

Unit V: Time Domain Performance [11 Hrs]

Zero Order, First Order and Second Order System – Unit Step Response and Ramp Response of First Order – Steady State Error for Ramp Response of Second Order – Hurwitz Roughs Stability Criterion – Procedure in Roughs Stability

TEXT BOOKS:

1. Muhammad Rashid, "Power Electronics Circuits, Devices and Applications", PHI II Edition, 1999 (Unit I, II & III)
2. M.S. Jamil Asghar " Power Electronics",PHI II Edition , (Unit I & II)
3. Katshiko Ogata, "Modern Control Engineering", Eastern Economy III Edition -1998 (Unit IV & V)

REFERENCE BOOK:

1. Sen, "Power Electronics", McGraw Hill International, VI Edition 1993
2. Power Elecrtonics: M.D.Singh,K.B.Khanchanani.

SEMESTER – I
MICROWAVE AND RADAR NAVIGATION SYSTEM
COURSE CODE: 15MEC103

Instructional hours per week: 5

Objective: To enable the students to learn the operations of microwave devices and circuits and also to get depth knowledge in RADAR and its Navigation Systems.

Unit I: Introduction to Microwave [12 Hrs]

Introduction – Maxwell's Equation – Ampere's Law – Faraday's Law – Gauss's law – Wave Equation – TEM/TE/TM/HE Wave Definitions – Wave Guide – Types of Wave Guides – propagation of Wave in the Rectangular Wave Guide – Propagation of TEM Waves – TE and TM Modes – Propagation of TM Waves in Rectangular Wave Guide

Unit II: Microwave Amplifiers and Oscillators [12 Hrs]

Klystron – Two Cavity Klystron Amplifier - Multi Cavity Klystron – Two Cavity Klystron Oscillator- Reflex Klystron – Traveling Wave Tube(TWT) – Applications – Backward Wave Oscillators – Magnetron: Cavity Magnetron – Sustained Oscillation of Magnetron

Unit III: Microwave Antennas [11Hrs]

Quantitative Theory of Short Dipole Antenna – Characteristics Grounded Quarter Wave and Ungrounded Half Wave Antenna – Radiation Resistance and Radiation Pattern – Folded Dipole Antenna and it's Applications – Arrays: Broad Side Array and End Fire Array – Loop Antenna – Direction Finding by Adhock Antenna – Rhombic Antenna – Horn Antenna – Parabolic Antenna

Unit IV: Principles of RADAR System [10 Hrs]

Radar Block Diagram and Operation - Radar Range Equation – Application of Radar System – Minimum Detectable Signal – Receiver Noise – Signal to Noise Ratio – Transmitter Power – Maximum Ambiguous Range

The Radar Receivers – Mixers – Duplexers – Displays

Unit V: FM RADAR and MTI Systems [10 Hrs]

Introduction to Doppler Effect – CW Radar – FM CW Radar – Multiple Frequency CW Radar – Moving Target Indicator(MTI) – Non Coherent MTI – Limitations of MTI Performance

Tracking with Radar – Sequential Lobbing – Conical Scan – Mono Pulse Tracking Radar – Comparison of Trackers

TEXT BOOKS:

1. N.Kulkarni, "Microwave and Radar Engineering", Umesh Publications, II Edition, 1999 (Unit I & II)

2. Scholnik, "Radar and Navigation", McGraw Hill Publications, II Edition 1980
(Unit IV & V)

3. K.D.Prasad, "Antenna and Propagation", Sathyapragasan Publication, VI Edition (Unit III)

SEMESTER – I
DIGITAL COMMUNICATION AND NETWORK TECHNIQUES
COURSE CODE: 15MEC104

Instructional hours per week: 5

Objective: To enrich the students to understand the basics of Digital Communication and Network techniques to develop their skill in the field of Digital Communication and network techniques.

Unit I: Introduction to digital communication systems [13 Hrs]

Communication Links – data communication system – synchronous and asynchronous data, binary data signal – serial Vs parallel communication

Pulse modulation: Sampling theory – PAM, PWM, PPM modulation and detection – time division multiplexing – frequency division multiplexing quantizing of analog signal — PCM principles – data modulation – ASK – FSK – PSK – DPSK

Unit II: Structure of Network Communication [10 Hrs]

Network Topologies – Fundamental of Communication Theory – Synchronizing Network Components – Communication Protocols –Categories of Networks- Internet Works- Transmission Mode

Unit III: Layer and Their Functions [13 Hrs]

OSI Reference Model – Physical Layer – Data Layer – Network Layer – Transport Session and application layer

MODEM: Modulation Techniques – Multilevel Transmission – Advance in Modem

SWITCHING: Circuit Switching – Message Switching – Compressing

Unit IV: LAN Network [9 Hrs]

LAN Definition – Major Components of LAN – Protocols – IEEE Standards – CSMA/CD – Token Ring –Token Bus – FDDI – Logical Link Control- Bridge-Router-Repeater-Gateway- HUB

Unit V: SONET/NETWORK SECURITY [10 Hrs.]

Synchronous Transport signals- Physical Configuration- SONET Layers- SONET Frame- Multiplexing sts frame, VLAN, VPN- Four Aspect of Security:- Privacy- Digital Signature- PGP- Access Authorization

TEXT BOOKS:

1. Prokis J J, "Digital Communication" TMH Pub Co Ltd, II Edition (Unit I)
2. A S. Tanenbaum, "Computer Networks" PHI Publisher (Unit II, III & V)
3. Ulysess Black, "Data Communication and Distributed Network", III Edition (Unit IV)

REFERENCE BOOK:

1. Behrouz A. Forouzan, " Data Communication and Networking", Tata McGraw Hill, New Delhi, 2000, II Edition

SEMESTER – I

PRACTICAL – I: 8051 MICROCONTROLLER AND ITS APPLICATIONS

COURSE CODE: 15MEC105

ANY TEN EXPERIMENTS:

1. Arithmetic and Logic Operations
2. Data transfer with parallel port
3. 8 channel quiz buzzer
4. Object Counter
5. Interfacing Matrix Keypad
6. LCD interface
7. A/D interface
8. D/A interface
9. Seven Segment display interface
10. Traffic light controller
11. Water level controller
12. Obstacle detector
13. Programmable timer
14. Serial interface
15. Digital clock

SEMESTER – I
PRACTICAL – II: ADVANCED ELECTRONICS
COURSE CODE: 15MEC106

ANY TEN EXPERIMENTS:

1. PAM Generation and Detection
2. LAN Network
3. Generation of PWM and PPM
4. FSK Generation and Detection
5. Control of Firing Circuits of Thyristor
6. An Optocoupler based gate driver to control AC Motor using Power MOSFET
7. Single Phase Inverter
8. Switching Circuits of TRIAC
9. Commutation Techniques of SCR
10. Regulator's Using Power BJT
11. Regulators Using Power MOSFET
12. Power Angle Control Circuit using SCR
13. Generation of PSK
14. Generation of ASK
15. Base Driver circuit to control DC Motor using Power BJT

SEMESTER II
EMBEDDED SYSYEM & RTOS DESIGN
COURSE CODE: 15MEC201

Instructional hours per week: 5

Objective: To enable the students to understand the various Embedded Real time operating systems and to study the architecture of PIC microcontroller and also to develop application using embedded system.

Unit I: Embedded Software Architecture& Operating System Services [10 Hrs]

Round Robin – Round Robin with Interrupts – Function Queue Scheduling Architecture – Real Time Operating Systems (RTOS) – Introductions to RTOS – Tasks and Data – Semaphores and Shared data- Message Queues, Mail box and Pipes – Timer Function – Events – Memory Management

Unit II: RTOS based Embedded System Design [10 Hrs]

OS Basics – Types of OS – Tasks, Process and threads- multiprocessing & multi tasking – Task Scheduling – Task communication – device driver- Choosing a RTOS

Unit II: Real time operating systems [10 Hrs]

VX works - μCOS II – POSIX standards - Salvo RTOS- RTOS Porting to a Target.

Unit IV: PIC CPU Architecture and Instruction Set [15 Hrs]

Overview – Harvard Architecture – Pipe lining – Program Memory considerations – Register like Structure and Addressing modes – CPU registers – Instruction Set – Simple Operations – External Interrupt and Timer – Overview RB0/INT External Interrupt Input Capture mode – Compare mode – Timer1/ CCP – Programming pre-scalar – Timer1 External Event counter – Timer1 and Sleep mode – PWM output – Port B Change Interrupts

Unit V: PIC Peripherals [10 Hrs]

Initialization and Programming of I2C bus for peripheral chip access – A/D Converters – UART – Serial Peripheral Interface – Special features.

TEXT BOOKS:

1. David E. Simon, "An Embedded Software Primer", Addison Wesley 2004 (Unit I)
2. Shibu KV "Introduction to Embedded system" Tata McGraw Hill 2010 (Unit II)
3. Micro C OS II reference manual, Salvo User manual & VX works Programmers manual. (Unit III)
4. Keil Real Time library documentation
5. PIC 16f877A Data Sheet (Unit IV & V)

REFERENCE BOOK

1. John .B. Peatmen, "Design with PIC Microcontroller", Pearson Education, LPE, II reprint 2002

SEMESTER – II
VHDL PROGRAMMING
COURSE CODE: 15MEC202

Instructional hours per week: 5

Objective: To enable the students to learn concept of VLSI design and to understand the various elements, behavior of VHDL programming language.

Unit I: Introduction to VHDL **[10 Hrs]**

Basic terminology – Design flow – VHDL objects – Entity declarations – Architectural body – Process declarations – Architectural body – Configuration – Functions – Procedures – Package declaration – Package body – Library

Unit II: Basic Language Elements **[10 Hrs]**

Identifiers – Data objects – Data types – Scalar – Integer – Enumerators – Physical – Floating point – Composite – array – Record – Access types – Incomplete types – File types.

Unit III: Operators, Generics and Configurations. **[10Hrs]**

Operators – Logical – Relational – Shift – Adding – Multiplying – Miscellaneous – Generics – Configurations specifications – Configuration declaration – Default rules – conversion function – Direct Instantiation.

Unit IV: Programming Model **[15 Hrs]**

Behavioral Modeling: Process Statement – Conditional Statement – IF, CASE, LOOP, NEXT and WAIT Statements, Assertion Statement – Exit Statement

Structural Modeling: Component declaration – Component instantiation – Signals – Variables – Delays – Inertial delay – Transport delay

Data Flow Modeling: Concurrent Statement – Concurrent versus Sequential Statement – Conditional Signal Assignment Statement

Unit V: Applications **[10 Hrs]**

VHDL representation: Decoders – Encoders – Multiplexers – De-multiplexers – Adder – Subtractor – Multiplier – Counters – Shift registers – Simple ALU –Pulse counter – Clock Divider – VGA Interfacing – UART interfacing.

TEXT BOOK:

1. J. Bhasker, "VHDL Primer" III Edition, PHI, Six impression 2007 (Unit I – V)

REFERENCE BOOKS:

1. Dougles L. Perry, "VHDL", III Edition, Tata McGraw Hill, 2002.
2. Moris Mano and Charles R. Kime, " Logic Circuit Layout and Design" II Edition, Pearson Education Asia, 2002

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SEMESTER – II

ELECTIVE – I: FIBER OPTIC COMMUNICATION

COURSE CODE: 15MEC203

Instructional hours per week: 5

Objective: To enable the students to understand the various concepts of fiber used in communication. It also helps them to learn the optic communications usage.

Unit – I **[12 Hrs]**

Optical fibers- Importance of optical fibers- propagation of light waves- basic structure of fiber and propagation of light in an optical fiber- acceptance angle and acceptance cone of a fiber- Numerical aperture- Fiber classification(Stepped index fiber, Stepped index mono mode fiber, Graded index multimode fiber)- Disadvantages of mono mode fiber- Numerical aperture of graded index fiber

Unit – II **[10 Hrs]**

Modes of propagation- Merdinal and Skew rays- Modes and cut off parameter of fibers- single mode propagation- Comparison of steps and graded index fiber- Optical fiber Vs cylindrical wave guide and its wave guide equations- Wave equation in step index fibers- Flow of power in step index fiber

Unit – III **[10 Hrs]**

Over view of attenuation- Attenuation units- Core and cladding loss- signal distortion in optical wave guide- Information capacity determination- Group delay- Materials- Dispersion- Wave guide dispersion- Inter modal dispersion- Pulse broadening in graded index guides. Measurement of NA value- Measurement of attenuation

Unit – IV **[10 Hrs]**

Source to fiber power launching- Source output pattern- Power coupling calculations- Power launching Vs wavelength- Equilibrium numerical aperture- Lensing scheme for coupling- Improvement imaging micro sphere- LASER diode to fiber coupling- Fiber losses- Fiber end face preparation- Splicing techniques

Unit – V **[13 Hrs]**

Optical sources: LED- Basic process involved in LED's- Output characteristics of LED- Fiber LED coupling- LASER- LASER operation. Optical detector: Characteristic of photo detector- Photo emissive photo detector(Phototubes and Photo multiplier)- Optical amplifier: Basic application- Optical amplifier types- Gain- Amplifier noise figure- Optical bandwidth. Optical switches: Photonic switching- Mechanical switching- Integrated optical switch. Applications: Military, Civil, Consumer and Industrial applications.

REFERENCE BOOK:

1.Subir Kumar Sarkar, "Optical Fibres and Optical Communication Systems", S. Chand& Company Ltd, 1997. [Unit I, II, III& V]

2.Gerd Keiser, "Optical Fibre Communication system", McGraw Hill II Edition, 1893 [Unit IV].

SEMESTER – II

ELECTIVE – I: HIGH PERFORMANCE COMMUNICATION NETWORKS

COURSE CODE: 15MEC203A

Instructional hours per week: 5

Objective: This paper enables the students to understand and to improve their practical knowledge in high performance communication networks.

UNIT – I: BASICS OF NETWORKS [13 Hrs]

Telephone, Computer, Cable Television And Wireless Network, Networking Principles, Digitalization – Service Integration, Network Services And Layered Architecture, Traffic Characterization And QOS, Network Services – Network Elements And Network Mechanisms

UNIT – II: PACKET SWITCHED NETWORKS [9 Hrs]

IP Models – Ethernet (IEEE 802.3), Token Ring (IEEE 802.5), FDDI, DQDB, and Frame Relay, SMDS – Internet Working With SMDS

UNIT – III: INTERNET AND TCP/IP NETWORKS [10 Hrs]

Overview – Internet Protocol – TCP And UDP – Performance Of TCP/IP Networks Circuit Switched Networks – SONET, DWDM, Fiber To Home, DSL, Intelligent Networks, CATV

UNIT – IV: ATM AND WIRELESS NETWORKS [11 Hrs]

Main Features – Addressing, Signaling And Routing, ATM Header Structure – Adaptation Layer, Management And Control BISDN, Interworking With ATM, Wireless Channel, Link Level Design, Channel Access, Network Design And Wireless Networks

UNIT – V: OPTICAL NETWORKS AND SWITCHING [12 Hrs]

Optical Links – WDM Systems, Cross-Connects, Optical LAN's, Optical Paths And Networks, TDS And SDS: Modular Switch Designs – Packet Switching, Distributed, Shard, Input And Output Buffers

TEXT BOOK:

1. Jean warland and pravin varaiya, "High performance communication networks", 2nd edition, Harcourt and Morgan Kauffman, London, 2000 (Unit I – V)

SEMESTER – II
ELECTIVE – I: ADVANCED SPEECH PROCESSING
COURSE CODE: 15MEC203B

Instructional hours per week: 5

Objective: This paper enhances the students to understand the basic concept of digital speech processing and to study the various applications of speech processing.

UNIT – I: **[13 Hrs]**

Digital Speech processing: Introduction to digital speech processing, digital transmission and storage of speech, speech synthesis, speaker verification and identification systems, speech recognition and aids to handicapped, speech production mechanism, Classification of speech sounds, Nature of speech signal, Models of speech production

UNIT – II: **[10 Hrs]**

Time domain methods for speech processing: Significance of short time analysis, Time domain parameter of speech: methods for extracting the parameters. Energy, magnitude, zeros crossing rates, Auto correlation function, pitch estimation – parallel processing

UNIT – III: **[9 Hrs]**

Frequency domain methods for speech processing: Short time Fourier analysis, Filter bank analysis, spectrographic analysis, format extraction, pitch extraction, analysis – synthesis systems

UNIT – IV: **[13 Hrs]**

Homomorphic analysis and LPC of speech: Cepstral analysis of speech format and pitch estimation, formulated of linear prediction problem in time domain: basic principle, autocorrelation methods, covariance methods, solutions of LPC equations: Cholesky decomposition, Durbin's recursive algorithm, Lattice formulation and solution, Comparison of different methods, Applications of LPC parameters

UNIT – V: **[10 Hrs]**

Applications of speech signal processing: Speech recognition – Specification of a typical application, voice response system. Algorithms: Spectral estimation, dynamic time warping, hidden markov model. Speech synthesis: Text to speech, voice over IP, Speaker verification and identification

TEXT BOOKS:

1. L.R. Rabiner and R.W.Schaffer: Digital processing of speech signals, Prentice Hall, 1978 (Unit I, II)
2. J.L.Flanagan: Speech analysis synthesis and perception, 2nd edition, Berlin, 1972 (Unit III, IV)
3. J.H.Witten: Principles of computer speech, Academic press, 1982 (Unit – V)

SEMESTER – II

PRACTICAL – III: EMBEDDED SYSTEM & RTOS LAB

COURSE CODE: 15MEC204

ANY TEN EXPERIMENTS:

1) Parallel port interface
2) Delay generation using hardware timer
3) External event counter using timer 1
4) Internal ADC programming
5) Speed control of DC motor using PWM module
6) Interfacing RTC using I^2C bus
7) Interfacing serial EEPROM
8) UART interface
9) LCD interface
10) Temperature monitoring and control
11) D/A interface
12) Traffic Light controller
13) Water level controller
14) RTOS Multitasking
15) RTOS ISR
16) Priority Inversion

SEMESTER – II

PRACTICAL – IV: VHDL PROGRAMMING

COURSE CODE: 15MEC205

ANY TEN EXPERIMENTS:

1) Implementation of Logic Gates
2) Half Adder and Full Adder Design
3) Half Sub tractor and Full Sub tractor Design
4) Encoder and Decoder design
5) Multiplexer and De-multiplexer
6) Implementation of PLA
7) Flip Flop and Latches
8) ALU Design
9) Shift Register and Ring Counter
10) Seven Segment Interface
11) PS/2 Keyboard interface
12) Clock Divider
13) RAM and ROM design
14) VGA Interface
15) Implementation of UART

SEMESTER – II

SUPPORTIVE COURSE – I: ANALYSIS AND PROCESSING OF SIGNALS

COURSE CODE:

Instructional hours per week: 5

Objective: This paper enables the students to understand the basic concepts of signals and system and also to enable them to analyze various techniques like FFT, DFT and processing of audio / video signals.

UNIT – I: **[10 Hrs]**

An Introduction to DSP and its application – Signals – Requirements for linearity – static linearity and sinusoidal fidelity – Examples of linear and non linear systems – Special properties of linearity – Superposition, The foundation of DSP – Common decomposition – Alternative to linearity

UNIT – II: **[10 Hrs]**

The delta functions and impulse functions – Convolution – Mathematical properties of convolution – Correlation – Speed – The input side algorithm – The output side algorithm – The sum of weighted inputs

UNIT – III: **[10 Hrs]**

The family of Fourier transforms – Notation and formula of the real DFT – DFT basic functions – Synthesis and analysis of DFT – Duality – Spectral analysis of signals – Frequency response of the systems – Convolution via the frequency domain

UNIT – IV: **[12 Hrs]**

Working Principle of FFT – Speed and precision comparison – Continuous signal processing: The delta function – The convolution – The Fourier transform – The Fourier series
Introduction to digital filters – Filter basics – Time domain parameters – Frequency parameters – High pass filters – Band pass filters – Band pass and Band rejection filters

UNIT – V: **[13 Hrs]**

Audio processing – Human hearing – Timbre – Sound quality Vs Data rate – High fidelity audio – Compounding – Speech synthesis and Recognition – Image formulation and Display: Digital image structure – Cameras and End Eyes – Television video signals – Other image acquisition and display – Brightness and contrast adjustments – Warping

TEXT BOOK:

1. Steven. W. Smith, "The Scientist and Engineers guide to DSP", California Technical Publishing, California, 1999 (Unit I – V)

REFERENCE BOOKS:

1. S. Salivahanan, "Digital Signal Processing", TMH publish limited, New Delhi, 2008
2. John. G. Proakis and dimities G. Manolaks, "Digital Signal Processing", PHI Publications, 2003

SEMESTER – II

SUPPORTIVE COURSE – I: NEURAL NETWORK AND ITS APPLICATIONS

COURSE CODE:

Instructional hours per week: 5

Objective: This paper enables the students to study and to get depth knowledge in the field of neural networks.

UNIT – I: INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS [10 Hrs]

Neuro – Physiology – General Processing Element – ADALINE – LMS learning rule – MADALINE – MR2 Training Algorithm

UNIT – II: BPN AND BAM [14 Hrs]

Back Propagation Network – Updating of output and hidden layer weights – Application of BPN – Associative memory – Bi-directional Associative Memory – Hopfield memory – Traveling salesman problem

UNIT – III: SIMULATED ANNEALING AND CPN [10 Hrs]

Annealing, Boltzmann machine – Learning – Application – Counter Propagation network – Architecture – Training - Applications

UNIT – IV: SOM AND ART [10 Hrs]

Self Organizing map – Learning algorithm – Feature map classifier – Applications – Architecture of Adaptive Resonance Theory – Pattern matching in ART network

UNIT – V: NEOCOGNITRON [11 Hrs]

Architecture of Neocognitron – Data processing and performance of architecture of spacio – Temporal networks for speech recognition

TEXT BOOKS:

1. J.A. Freeman and B.M.Skapura, "Neural Networks, Algorithms Applications and Programming Techniques", Addision – Wesely, 1990 (Unit – III, IV, V)
2. Laurene Fausett, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Prentice Hall, 1994 (Unit – I, II)

SEMESTER – II

SUPPORTIVE COURSE – I: ROBOTICS AND AUTOMATION

COURSE CODE:

Instructional hours per week: 5

Objective: This paper enrich the students and to understand the basic concepts of robotics organization and to develop new application using it.

UNIT – I: ROBOT ORGANIZATION [10 Hrs]

Coordinate transformation, Kinematics and inverse Kinematics, Trajectory planning and remote manipulation.

UNIT – II: ROBOT HARDWARE [13 Hrs]

Robot sensors – Proximity sensors – Range sensors – Visual sensors – Auditory sensors – Robot manipulators

Manipulator dynamics – Manipulator control – Wrists – End efforts – Robot grippers

UNIT – III: ROBOT AND ARTIFICIAL INTELLIGENCE [10 Hrs]

Principles of AI – Basics of learning – Planning movement – Basics of knowledge representations – Robot programming languages

UNIT – IV: ROBOTIC VISION SYSTEMS [11 Hrs]

Principles of edge detection – Determination optical flow and shape – Image segmentation – Pattern recognition – Model directed scene analysis

UNIT – V: ROBOT CONTROL AND APLLICATIONS [11 Hrs]

Robot control using voice and infrared – Overview of robot applications – Prosthetic devices – Robots in material handling, processing assembly and storage

TEXT BOOKS:

1. Vokopravotic, "Introduction to Robotics", Springer, 1988 (Unit – I)
2. Rathmill K., "Robot Technology and Application", Springer, 1985 (Unit – II)
3. Charniak & McDarmott, "Introduction to Artificial Intelligence", McGraw Hill, 1986 (Unit -III)
4. K.S.Fu, R.C.Gonzally, C.S.G.Lee, "Robotics Control, Sensing, Vision and Intelligence", McGraw Hill Book Company, 1997 (Unit – IV)
5. Mikell P. Groover, Mitchell Weiss, Roger. N, Nagel, Nicholas G. Odrey, "Industrial Robotic Technology Programming and Applications", McGraw Hill Book Company, 1986 (Unit – V)

SEMESTAR – III

ANALOG DEVICE BLACKFIN DSP
COURSE CODE: 15MEC301

Instructional hours per week: 5

Semester	III
Credit	5
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to learn the architecture of Analog Devices BLACKFIN 535 processor and to know the operation of peripherals present in it

UNIT I: INTRODUCTION TO ADSP-BF535 [13]

Introduction – ADSP – BF535 Core architecture – Memory Architecture – Internal and External Memory – Operating Modes and Status – User mode – Supervisor mode – Emulation mode – Idle state – Reset state – Booting Methods, Computational unit –Register files – ASTAT – ALU – MAC - Barrel Shifters

UNIT II: CHIP BUS HIERARCHY [9]

Chip bus hierarchy – Internal Interfaces – Core overview – System overview – System Interface

UNIT III: PCI INTERFACE AND USB [13]

PCI Specification – PCI device function – PCI host function – Processor core access to PCI space – External, PCI requirements – Device mode operations – Host mode operations.

USB Device – Convention and requirements – Block diagram – Features and modes

UNIT IV: PROGRAMMABLE FLAGS, TIMERS AND SERIAL PORTS [9]

Programmable Flags MMR Timer – General Purpose Timer – General Purpose Timer Registers – Timer modes – Core Timer – Watchdog Timer – Operation of SPI and S PORT Peripherals

UNIT V: RTC, EBIU and UART [11]

RTC Programming Model – Interrupts – RTC MMR s External bus interface unit – Block diagram – Internal memory interface – External memory interface – EBIU programming model – SDRAM Controller

UART – Serial Communication – Non DMA mode – DMA mode – IRDA Support.

TEXT BOOK:

1. ADSP-BF535 Black Fin Processor Hardware Reference Manual, Analog Devices Inc 2014 (Unit I – V)

SEMESTER – III
DIGITAL SYSTEM DESIGN USING VERILOG
COURSE CODE: 15MEC302

Instructional hours per week: 5

Semester	III
Credit	5
Max. Marks	CIA -25 CE -75 TOT =100

Objective: This paper enables the students to learn the statements, modeling structures and data types. It also motivates them to develop the programming skills to design a digital system.

UNIT 1: DIGITAL DESIGN WITH VERILOG HDL [14]

Evolution of CAD - Emergence of HDLs, Typical HDL- based design flow, Trends in HDLs - Hierarchical Modeling Concepts - Design methodology-modules and instances-parts of a simulation - design block - stimulus block. Basic Concepts - Lexical conventions - data types - system tasks, compiler directives.- Modules and Ports- Module definition, port declaration, connecting ports, hierarchical name

UNIT II: GATE LEVEL MODELING & DATA FLOW MODELING [11]

Gate-Level Modeling: Gate Types – Gate Delays – Examples, Dataflow Modeling: Continuous Assignments – Delays – Expressions, Operators and Operands – Operator Types

UNIT III: BEHAVIORAL MODELING [9]

Behavioral Modeling: Structured procedures- procedural assignments, Procedural - Assignments, Timing Control - Conditional statements - Multiway branching – Loops - sequential and parallel blocks - Tasks and Functions differences between tasks and functions - declaration, invocation - automatic tasks and functions. Examples

UNIT IV: ADVANCED VERILOG TOPICS [10]

Advanced Verilog Topics: Timing and delays-Types of delay models – path delay modeling – Timing Checks – Delay back annotation – Switch level modeling Elements – UDP basics – Combinational UDP Definition – Sequential UDP – UDP table shorthand symbols – Guidelines for UDP Design - Examples

UNIT – V: APPLICATIONS [11]

FSM - Modeling Examples – Modeling Combinational Logic – Modeling sequential logic – modeling a memory – Modeling Boolean equations – Modeling a Ripple counter – Modeling a full adder with carry look ahead – Modeling a parameterized comparator – Modeling a decoder – Modeling a multiplexer.

TEXT BOOKS:

1. Samir Planitkar “Verilog HDL” Second Edition IEEE 1364-2012 Compliant (Unit I - IV)
2. Douglas J Smith “ HDL Chip Design” Doone Publications, Second Edition,2012 (Unit V)

REFERENCE BOOKS:

1. J.Bhasker, “Verilog HDL Synthesis, A Practical Primer”, BS Publication, 3rd Edition, 2009

2. Micheal D. Ciletti, “Advanced Digital Design with the Verilog HDL”, PHI publications, Indian reprint, 2011

SEMESTER – III
ELECTIVE – II: ARM9 EMBEDDED PROCESSOR& RASPBERRY Pi
COURSE CODE: 15MEC303

Instructional hours per week: 5

Semester	III
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to understand & learn the architecture of ARM9 CPU with the Raspberry and explore their knowledge in embedded field.

UNIT – I: SAMSUNG S3C2440A ARM9 PRODUCT VIEW [13]

Introduction – Features – Block diagram –Pin assignments – Signal Descriptions Programmers model – processor operating states – Switching state – Memory Format –Big and Little Indian – Instruction length – operating modes – Exceptions – Reset

UNIT – II: VARIOUS INTEGRATED CONTROLLERS [10]

Memory controllers: - Overview – functional descriptions – Nand Flash Controllers: - Features – Boot loader function – pin configuration – Nand Flash configuration table – Software modes – USB controllers

UNIT – III: PERIPHERAL INTEGRATION [10]

Basic Timer: - Features – PWM Timer operation - I/O Port control description – Watchdog timer – Functional description of clock and Power management – DMA Operation – LCD Controller – STN LCD Controller operation – ADC and Touch screen interface operation

UNIT – IV: SERIAL INTERFACE [10]

UART – Features – Block diagram and operation – MMC/SD/SDIO controller:- Features – Block diagram and SDIO Operation – IIC Bus interface – overview and operation – SPI – Features , Block diagram and operation- Camera Interface- AC97 Controller

UNIT – V: RASPBERRY PI & APPLICATION [12]

Raspberry pi Setup and Management.- Operating system- software on raspberry pi – GPIO - Controlling of Hardware- Digital inputs – sensors – Displays

TEXT BOOK:

1. S3C2440A 32 bit CMOS Microcontroller user manual from Samsung, 2014(Unit I – IV)

2. Raspberry Pi Cookbook by Simon Monk, O'Reilly publication, December 2013 First Edition (Unit V)

SEMESTER – III
ELECTIVE – II: ANALYSIS AND DESIGN OF ANALOG IC's
COURSE CODE: 15MEC303A

Instructional hours per week: 5

Semester	III
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to learn about various analog ICs and to design applications using it

UNIT – I: CIRCUIT CONFIGURATION FOR LINEAR IC [13]

Current sources, analysis of difference amplifiers with active load, supply and temperature independent biasing techniques, voltage references

UNIT – II: OPERATIONAL AMPLIFIERS [11]

Analysis of Operational amplifier circuits, slew rate model and high frequency analysis, operational amplifier noise analysis and low noise operational amplifiers

UNIT – III: ANALOG MULTIPLIER AND PLL [11]

Analysis of four quadrant and variable Tran conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL

UNIT – IV: MOS ANALOG ICs [10]

Design of MOS Operational Amplifier, CMOS voltage references, MOS Power amplifier and analog switches

UNIT – V: MOS SWITCHED CAPACITOR FILTERS [10]

Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC Filters.

TEXT BOOKS:

1. Gray and Meyer, "Analysis and Design of Analog ICs", Wiley International, 2008 (Unit I)
2. Gray, Wooley, Brodersen, "Analog MOS Integrated Circuits", IEEE Press, 2007 (Unit II)
3. Kenneth R. Laker, Willy M.C. Sansen, William M.C.Sansen, "Design of Analog Integrated Circuits and Systems", Tata McGraw Hill, 2000 (Unit III, IV)
4. Behzad Razavi, "Principles of Data Conversion System Design", S. Chand & Company Ltd, 2004 (Unit V)

SEMESTER – III
ELECTIVE – II: ADVANCED NETWORK TECHNIQUES
COURSE CODE: 15MEC303B

Instructional hours per week: 5

Semester	III
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to understand the various concepts of Network techniques used in communication. It also helps them to learn advanced network communication usage.

Unit – I: Introduction to Network Communication [12]

Introduction – Network Transfer Capacity, Public and Private Network, Switched and Board Networks

Unit – II: Network Components [10]

Connecting Networks – Physical Interface – Transmission path – Wire pars – Coaxial – cables – Submarine cable – Comparison of wire pair cable and coaxial cable

Unit – III: Distributed Network Architecture [10]

Introduction – Architecture and Protocols – Layered Protocols – Open System Interconnections – Other OSI Standards

Unit – IV: LAN Hardware and Components [10]

Digital Network: Signal Conversion – Digital Carrier System – Channel and Data Services Units – ISDN – Narrow and Broad Band ISDN – Switches and HUBS – Bridges – Routers – Structured Cabling

Unit – V: Network Database Design Consideration [13]

Introduction – Ration Analysis – Data Base Design Decision Trees – Synchronous of Network Data bases – Additional Consideration on using Personal Computers

TEXT BOOK:

1. Ulysess Black, "Data Communication Distributed Network", 4th Edition, 2010 (Unit I,II,III & V)

2. A.S. Tanenbaum, "Computer Networks", PHI, 4th Edition, 2009 (Unit VI)

Reference Book:

1. Beherouz A.Forouzan, "Data Communication and Networking", Tata McGraw Hill, 4th Edition, 2014

SEMESTER – III
PRACTICAL – V: ANALOG DEVICE BLACKFIN DSP
COURSE CODE: 15MEC304

Semester	III
Credit	3
Max. Marks	CIA -40 CE -60 TOT =100

ANY TEN EXPERIMENTS:

1. DSP special arithmetic and logical operations
2. Generation of signals using MATLAB
3. Key Board/ LED Interface via programmable flags using ADSP kit
4. Convolution of discrete signals using MATLAB
5. Correlation of discrete signals using MATLAB
6. Generation of AM using MATLAB
7. Generation of DFT using MATLAB
8. FIR filter design using ADSP kit
9. A-law compression and expansion using ADSP kit
10. Voice encoding and decoding using codec using ADSP kit
11. RTC programming using ADSP kit
12. Programming Timer using ADSP kit
13. SPI peripheral interface using ADSP kit
14. UART interface using ADSP kit
15. Data transfer using programmable Flags

SEMESTER III
PRACTICAL – VI: VERILOG HDL PROGRAMMING
COURSE CODE: 14MEC305

Semester	III
Credit	3
Max. Marks	CIA -40 CE -60 TOT =100

ANY TEN EXPERIMENTS:

1. Verification of logic gates with test bench
2. Generation of signals such as sine, square, triangular wave with test bench
3. Four bit full adder and Subtractor in single module with test bench
4. Encoder and decoder with test bench
5. Multiplexer and Demultiplexer with test bench
6. Flip flop and latches with test bench
7. Design a 2 bit Micro Processor with test bench
8. Memory Module both synchronous and asynchronous – RAM, ROM
9. Design a Finite state Machine and check the result with help of test bench
10. Design a synchronous and asynchronous Clock divider and generation
11. Interfacing of Seven Segment in Spartan 3 development kit
12. Interfacing of key board in Spartan 3 development
13. Interfacing of VGA in Spartan 3 development
14. Interfacing of UART in Spartan 3 development
15. Digital Clock design using Xilinx ISE Project Navigator

Inter Department Course Subject to be offered by Other Department

FUNDAMENTALS OF EMBEDDED SYSTEMS

Semester	III
Credit	3
Max. Marks	CE -100 TOT =100

UNIT – I: ARCHITECTURE OF EMBEDDED SYSTEMS

Categories of Embedded Systems - Specifications of Embedded systems - Recent trends in Embedded Systems - Hardware Architecture - Software Architecture - Communication software - Process of generation of executable image – development /testing tools

UNIT – II: PROGRAMMING FOR EMBEDDED SYSTEMS

Getting the most of C - data types - manipulating bits in memory and I/O ports - accessing memory mapped I/O devices - structures - variant access - mixing C to assembly - register usage - use of addressing options - instruction sequencing - procedure call and return - parameter passing - retrieving parameters memory management - scope - automatic allocation - static allocation - dynamic allocation - shared memory - recognizing shared objects - re-entrant functions - accessing shared memory device drivers – productivity tools

UNIT – III: HARDWARE PLATFORM

PIC microcontroller - Architecture of PIC 16c6x/7x- FSR - Reset action - Oscillatory connection – Memory organization - Instructions - Addressing modes - I/O ports - Interrupts - Timers - ADC- Assembly language programming

UNIT – IV: REAL-TIME OPERATING SYSTEM CONCEPTS

Architecture of the Kernel - task and task scheduler - Interrupt Service Routines - Semaphores - Mutex Mailboxes - Message Queues - Event Registers - Pipes - Signals - Timers - Memory Management – Priority Inversion Problem

UNIT – V: REAL-TIME OPERATING SYSTEM TOOLS AND CASE STUDIES

Use of μC/OS - II - Case study of coding for an Automatic Chocolate Vending Machine using MUCOS RTOS - Case study of an Embedded system for an Adaptive Cruise Control Systems in a Car - Case study of an Embedded Systems for a Smart Card

TEXT BOOKS:

1. Prasad K.V.K.K, “Embedded/Real Time Systems: Concepts, Design and Programming”, Dream tech, Wiley 2003.
2. Daniel W Lewis, “Fundamentals of Embedded Software”, Pearson Education, 2001.
3. Ajay V Deshmukh, “Microcontroller Theory and Applications”, Tata McGraw Hill, 2005.

REFERENCE BOOKS:

1. David E Simon, “An Embedded Software Primer”, Pearson Education, 2003.
2. Raj Kamal, “Embedded Systems Architecture Programming and Design”, Pearson, 2005.
3. Peatman, “Designing with PIC Micro Controller”, Pearson 2003.

SEMESTER – III

Supportive Course – II: MOBILE COMMUNICATION SYSTEMS & STANDARDS

COURSE CODE:

Instructional hours per week: 5

Semester	III
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to learn the various mobile communication system and standards and excel in mobile communication system

UNIT – I: INTRODUCTION TO MOBILE COMMUNICATION SYSTEMS [10]

Evolution of Mobile radio communications – Mobile radio systems in the U.S. and around the world – Examples of Mobile radio systems.

UNIT – II: CELLULAR CONCEPT [10]

Cellular concept – Frequency reuse – Channel Assignment strategies – Handoff strategies – Interference and System capacity – Trunking and Grade of service – Improving capacity in cellular systems.

UNIT – III: MOBILE RADIO PROPAGATION [10]

Small-scale multipath propagation – Impulse response of a multipath channel – Parameters of mobile multipath channel – Types of small-scale fading – Rayleigh and Rician distributions – Statistical models for multipath fading channels.

UNIT – IV: GSM, GPRS, 3G STANDARDS [10]

GSM services and features – GSM system architecture – GSM radio subsystem – Frame structure for GSM – Signal processing in GSM – GPRS network architecture – GPRS services and features – 3G UMTS network architecture – UMTS services and features.

UNIT – V: MULTIPLE ACCESS TECHNIQUES AND WIRELESS NETWORKING [15]

Multiple access techniques – FDMA, TDMA, TDMA/FDD, CDMA, SDMA and OFDMA/MIMO/SC-FDMA, MIMO/SOFDMA, OFDM/MIMO, HCSDMA/TDD/MIMO – Wireless networking – Design issues in personal wireless systems – Cordless systems and Wireless Local Loop (WLL) – IEEE 802.16 Fixed Broadband Wireless Access standard, WIMAX, HSPA, LTE and LTE Advanced standards – Mobile IP and Wireless Application Protocol.

REFERENCES

1. Rappaport, T.S., "Wireless Communications, Principles and Practice", 2ndEdition, Prentice Hall, NJ, 2009.

2. William Stallings, "Wireless Communications and Networks", 2ndEdition, Pearson Education, 2009.

3. Siegmund M. Redl, Mathias K. Weber, Malcolm W. Oliphant, "An Introduction to GSM", Artech House Publishers,1998

SEMESTER – III
Supportive Course – II: DIGITAL IMAGE PROCESSING
COURSE CODE:

Instructional hours per week: 5

Semester	III
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to learn about images and systems and also to understand the concepts of image processing, restoration and compression techniques.

UNIT – I: CONTIUOUS AND DISCRETE IMAGES AND SYSTEMS [13]

Light, Luminance, Brightness and Contrast, Eye, The Monochrome Vision Model, Image Processing Problems and Applications, Vision Camera, Digital Processing System, 2-D Sampling Theory, Aliasing, Image Quantization, Lloyd Max Quantizer, Dither, Color Images, Linear Systems And Shift Invariance, Fourier Transform, Z-Transform, Matrix Theory Results, Block Matrices and Kronecker Products.

UNIT – II: IMAGE TRANSFORMS [8]

2-D orthogonal and Unitary transforms, 1-D and 2-D DFT, Cosine, Sine, Walsh, Hadamard, Haar, Slant, Karhunen-loeve, Singular value Decomposition transforms.

UNIT – III: IMAGE ENHANCEMENT [13]

Point operations - contrast stretching, clipping and thresholding density slicing, Histogram equalization, modification and specification, spatial operations - spatial averaging, low pass, high pass, band pass filtering, direction smoothing, medium filtering, generalized cepstrum and homomorphic filtering, edge enhancement using 2-D IIR and FIR filters, color image enhancement.

UNIT – IV: IMAGE RESTORATION [8]

Image observation models, sources of degradation, inverse and Wiener filtering, geometric mean filter, non linear filters, smoothing splines and interpolation, constrained least squares restoration.

UNIT – V: IMAGE DATA COMPRESSION AND IMAGE RECONSTRUCTION FROM PROJECTIONS [13]

Image data rates, pixel coding, predictive techniques transform coding and vector DPCM, Block truncation coding, wavelet transform coding of images, color image coding. Random transform, back projection operator, inverse random transform, back projection algorithm, fan beam and algebraic restoration techniques.

TEXT BOOKS:

1. Anil K.Jain, "Fundamentals of Digital Image Processing", PHI, I Edition, 2007 (Unit I)
2. M.A.Sid Ahmed ,"Image Processing", McGraw Hill, Inc, 2006 (Unit II,III)
3. R.Gonzalaz and E.Woodes, "Digital Image Processing", Addison Wesley, II Edition, 2009 (Unit IV)
4. William. K.Pratt, "Digital Image Processing", Wiley Interscience, II Edition, 2007 (Unit V)

SEMESTER – III

Supportive Course – II: MULTIMEDIA COMPRESSION TECHNIQUES

COURSE CODE:

Instructional hours per week: 5

Semester	III
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: This paper enables the students to understand the concept of compression techniques in multimedia and various protocols used in multimedia.

UNIT – I: INTRODUCTION [13]

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video

UNIT – II: SUBNETWORK TECHNOLOGY [12]

Broadband services, ATM and IP, IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance

UNIT – III: MULTICAST AND TRANSPORT PROTOCOL [10]

Multicast over shared media network, multicast routing and addressing, scalping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP

UNIT – IV: MEDIA - ON – DEMAND [10]

Storage and media servers, voice and video over IP, MPEG-2 over ATM/IP, indexing synchronization of requests, recording and remote control

UNIT – V: APPLICATIONS [10]

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy

TEXT BOOKS:

1. Jon Crowcroft, Mark Handley, Ian Wakeman, “Internetworking Multimedia”, Harcourt Asia Pvt.Ltd.Singapore, 2006 (Unit I)

2. B.O. Szuprowicz,” Multimedia Networking”, McGraw Hill, NewYork, I Edition, 2001 (Unit II, III)

3. Tay Vaughan, “Multimedia making it to work”, Tata McGraw-Hill, IV Edition, NewDelhi, 2004 (Unit IV, V)

SEMESTAR – IV
MEMS and NEMS
COURSE CODE: 14MEC401

Instructional hours per week: 5

Semester	IV
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to learn about various materials used in MEMS and NEMS. This paper also helps them to study the operation of various MEMS sensors, fabrication process and their applications.

UNIT I: OVERVIEW OF MEMS & WORKING PRINCIPLES OF MICROSYSTEM [15]

Mems as Micro sensor-Micro actuator- Microsystems products –Comparison of Microsystems and Microelectronics – Multi disciplinary nature of Microsystems design and manufacturing – Applications of Microsystems

Micro sensors: Bio medical and Biosensor– Chemical Sensor – Thermal sensor

Micro Actuation: Actuation by Thermal Forces, Shape Memory Alloys, Piezo Electric Crystals and Electrostatic Force-Micro motors –Micro valves – Micro pumps- Micro Accelerometer.

UNIT II: MATERIALS FOR MEMS [10]

Substrates And Wafer – Czochralski method for growing single crystal- Crystal structure– Silicon Compounds – Silicon Dioxide – Silicon Carbide –Silicon Nitride – Poly Crystalline Silicon-Polymers –The Longmuir Blodgett (LB) Film

UNIT III: MICROSYSTEM FABRICATION PROCESS [10]

Photolithography – Ion Implantation – Diffusion – Oxidation –CVD-PVD– Sputtering – Deposition by Epitaxy – Etching.

UNIT IV: MICROMANUFACTURING AND MICRO SYSTEM DESIGN [10]

Micro Manufacturing: Bulk Micro Manufacturing – Surface Micro Machining – The LIGA process

Microsystems Design **:** Design consideration –Computer Aided Design (CAD)

UNIT V: NEMS PROPERTIES AND APPLICATION [10]

Properties of Nano material: Mechanical properties-Melting of Nano particles- Electrical conductivity-Optical properties

Applications: Electronics- Automobiles-Domestic appliances-Bio-technology and Medical field-Space and Defense.

TEXT BOOKS:

1. Tai – Ran Hsu, " MEMS and Microsystems Design and Manufacture " Tata McGraw Hill Edition 2002, ISBN 0 – 07-048709- X (Unit I – V)

REFERENCE BOOKS:

1. Sulabha K. Kulkarni, "Nano technology: principles and practices" Capital publishing company
2. P.K. Sharma, "Understanding Nano Technology", Vista Publications, I Edition, 2008

SEMESTAR – IV
AUTOMOTIVE EMBEDDED SYSTEMS
COURSE CODE: 14MEC402

Instructional hours per week: 5

Semester	IV
Credit	4
Max. Marks	CIA -25 CE -75 TOT =100

Objective: To enable the students to understand the various architecture and technologies used in automotive vehicles. It also helps them to learn the embedded communications used in Automotives.

UNIT-I: AUTOMOTIVE ARCHITECTURE [11]

General Context - Functional domains-Standardized components, Models and Processes – Certification Issue of safety critical In Vehicle embedded systems

UNIT-II: INTELLIGENT VEHICLE TECHNOLOGIES [10]

Road transport and its evolution – New technologies – Dependability Issues – Autonomous Car

UNIT-III: AUTOMOTIVE PROTOCOLS [10]

Automotive communication Systems Characteristics and constraints – InCar Embedded Networks – Middleware Layer – Open issues for Automotive Communication Systems

UNIT-IV: EMBEDDED COMMUNICATIONS [15]

FLEX RAY

Introduction - Event driven verses Time driven communication-Objectives of flex ray-Flex ray communication-Frame format -Communication cycle-Static segment-Dynamic segment

FLEX CAN

Main requirements of Automotive Networking - Network technologies- CAN features and limitations-Control system - Flex CAN architecture-Flex CAN address CAN limitations-Flex CAN applications

UNIT – V EMBEDDED SOFTWARE: **[9]**

Product Lines in Automotive Electronics

Characteristics of Automotive Product Lines – Basic Technology – Global Coordination of Automotive Product line variability – Artifact level variability

TEXT BOOK:

1. NICOLAS NAVET, FRANCAISE SIMONOT –LION, “Automotive Embedded Systems Hand Book” , CRC Press 2009 (Unit I – V)