S.N.R.SONS COLLEGE (AUTONOMOUS)
DEPARTMENT OF ELECTRONICS
M.Sc., APPLIED ELECTRONICS
WITH SPECIALIZATION IN VLSI SYSTEM DESIGN
(ACADEMIC YEAR 2014 – 2015 ONWARDS)
SCHEME OF EXAMINATION

SEMESTER I:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	14MEV101	Microcontroller Design, Programming and Applications	5	3	25	75	100
2	14MEV102	Power Electronics and Control Systems	4	3	25	75	100
3	14MEV103	Introduction to VLSI Design	4	3	25	75	100
4	14MEV104	VLSI Design Using VHDL	4	3	25	75	100
5	14MEV105	**Practical I:** VLSI System Design using VHDL Programming	3	4	40	60	100
6	14MEV106	**Practical II:** Microcontroller Programming and It Applications	3	4	40	60	100
		TOTAL	**23**				**600**

SEMESTER II:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	14MEV201	VLSI Design Using Verilog	4	3	25	75	100
2	14MEV202	Embedded System & Real Time Operating System Design	5	3	25	75	100
3		**Supportive Course - I**	4	3	25	75	100
4	14MEV203 / 14MEV203A / 14MEV203B	**Elective – I**	4	3	25	75	100
5	14MEV204	**Practical III:** VLSI Design using Verilog	3	4	40	60	100
6	14MEV205	**Practical IV** Embedded System & RTOS Lab	3	4	40	60	100
		TOTAL	**23**				**600**

SEMESTER III:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	14MEV301	ASIC Design	5	3	25	75	100
2	14MEV302	TI TMS 320C54X DSP	5	3	25	75	100
3		**Supportive Course – II**	4	3	25	75	100
4	14MEV303 / 14MEV303A / 14MEV303B	**Elective – II**	4	3	25	75	100
5	14MEV304	**Practical V:** Advanced VLSI System	3	4	40	60	100
6	14MEV305	**Practical VI:** TI TMS320C54X DSP	3	4	40	60	100
		TOTAL	**24**				**600**

SEMESTER IV:

S.No	Course Code	Course	Credit	Exam Hours	CIA	CE	Total
1	14MEV401	MEMS and NEMS	4	3	25	75	100
2	14MEV402	Automotive Embedded Systems	4	3	25	75	100

S.No	Course Code	Course	Credit	Project Report	Viva Voce	Total
3	14MEV403	Project Work and Viva – voce	12	160	40	200
		TOTAL	**20**			**400**

CIA – CONTINUOUS INTERNAL ASSESSMENT

CE – COMPREHENSIVE EXAMINATION

SUPPORTIVE COURSE:

S.No	SUPPORTIVE COURSE – I	SUPPORTIVE COURSE – II
1	Analysis and processing of signals	System Verilog
2	Robotics and Automation	Digital Image Processing
3	Neural Network and Its Application	Multimedia Compression Techniques

ELECTIVE:

S.No	Course Code	Elective – I	Course Code	Elective – II
1	14MEV203	Algorithm for VLSI Design Automation	14MEV303	Arm9 core Embedded Processor
2	14MEV203A	High performance communication network	14MEV303A	Analysis and design of analog IC'S
3	14MEV203B	Analog VLSI Design	14MEV303B	Mobile computing

Total Marks: 2200

Total Credits: 90

CONTROLLER OF EXAMINATIONS ★ SNR SONS COLLEGE, CBE-6 ★

Prof. G. SENTHIL KUMAR
Chairman, Board of studies in Electronics
S.N.R. Sons College, Coimbatore

SEMESTER – I

MICROCONTROLLER DESIGN PROGRAMMING AND APPLICATIONS

COURSE CODE: 14MEV101

Instructional hours per week: 5

Objective: To enhance the students to understand the working principles of microcontroller and to get wide knowledge in the field of 8051 microcontroller and its applications.

Unit I: Microprocessor and Microcontroller **[11 Hrs]**

Introduction – Microprocessor and Microcontrollers – A Microcontroller Survey – The 8051 Architecture – 8051 Microcontroller Hardware – 8051 data types and directives - Introduction and structure of assembly language

Unit II: Instruction Set **[10 Hrs]**

Addressing Modes – Data Transfer Instruction – Logical Instruction– Arithmetic Instructions – Jump and Call Instructions

Unit III: Microcontroller Design **[12 Hrs]**

Microcontroller Design: External Memory and Memory Spacing Decoding – Reset and Clock Circuits – Expanding I/O – Memory Mapped I/O – Memory Access Time

Testing the Design: Crystal Test – ROM Test and RAM Test – Time delay generation and calculation – Lookup Tables For The 8051

Unit IV: Timer/Counter, Serial Communication and Interrupt Programming **[13 Hrs]**

Timer / Counter Programming in the 8051: Programming 8051 Timers - Counter Programming

Serial Communication: Basic Serial Communication – 8051 Connection to RS232 – 8051 Serial Communication Programming

Interrupt Programming: 8051 Interrupts – Programming Timer Interrupts – Programming Hardware External Interrupts – Programming the Serial Communication Interrupt Priority in The 8051

Unit V: Applications **[9 Hrs]**

Interfacing an LCD - ADC interface, Interfacing Temperature Sensor – Interfacing a Stepper Motor - Interfacing to the Keyboard - Interfacing a DAC

TEXT BOOKS:

1. Kenneth J. Ayala, "The 8051 Microcontroller Architecture, Programming and Application", Penram International Publications, Second Edition (Unit I – V)

2. Muhammad Ali Mazidi, Janice Gillispie Mazidi, "The 8051 Microcontroller and Embedded Systems", Pearson Education, LPE 8th reprint 2004

SEMESTER – I
POWER ELECTRONICS AND CONTROL SYSTEMS
COURSE CODE: 14MEV102

Instructional hours per week: 5

Objective: To enable the students to understand the basic concepts of power controlled circuits and to learn various parameter in control system engineering

Unit I: Power Semiconductors **[12 Hrs]**

Construction and Operations of SCR, UJT and TRIAC – Thyristor Communication Techniques: Introduction – Natural Commutation – Forced Commutation – Self Commutation – Impulse Commutation – Response Pulse Commutation – External Pulse Commutation – Load Side and Line Side Commutation – Complementary Commutation

Unit II: Choppers **[10 Hrs]**

DC Choppers: Introduction – Principle of Step down Operation – Step Down with RL Load – Principle of Step Up Operation

Switch Mode Regulators: Buck Regulators – Boost Regulators – Buck/Boost Regulators – CUK Regulation – SMPS

Unit III: Invertors and switches **[11 Hrs]**

Invertors: Introduction – Principle of Operations – Single Phase Bridge Invertors – Three Phase Invertors

AC Voltage Controller: Introduction – Principle of ON/OFF Control – Principle of Phase Control

Static Switches: Introduction – Single Phase and Three Phases AC Switches – DC Switches – Solid State Relays

Unit IV: Control System and Feedback Characteristics **[11 Hrs]**

Open Loop and Closed Loop System – Classification of Control System – Transfer Functions - Block Diagram Reduction Rules – Signal Flow Graph – Manson's Gain Formula – Advantages and disadvantages of Open loop System

Unit V: Time Domain Performance **[11 Hrs]**

Zero Order, First Order and Second Order System – Unit Step Response and Ramp Response of First Order – Steady State Error for Ramp Response of Second Order – Hurwitz Roughs Stability Criterion – Procedure in Roughs Stability

TEXT BOOKS:

1. Muhammad Rashid, "Power Electronics Circuits, Devices and Applications", PHI II Edition, 1999 (Unit I, II & III)

2. Katshiko Ogata, "Modern Control Engineering", Eastern Economy Edition – 3rd Edition-1998 (Unit IV & V)

REFERENCE BOOK:

1. Sen, "Power Electronics", McGraw Hill International, VI Edition 1993

SEMESTER – I
INTRODUCTION TO VLSI DESIGN
COURSE CODE: 14MEV103

Instructional hours per week: 5

Objective: This paper enables the students to learn about the various technologies used in VLSI Design process and it gives a basic knowledge in hardware description language.

Unit I: VLSI Design [12 Hrs]

A Brief History - MOS Transistors - CMOS Logic - CMOS Fabrication and Layout - Design Partitioning - Logic Design - Circuit Design - Physical - Design Verification - Fabrication, Packaging, and Testing MOS transistor theory - Introduction Long - Channel I-V Characteristics - Nonideal I-V - DC Transfer Characteristics - Pitfalls and Fallacies

Unit II: CMOS Processing Technology [12 Hrs]

Introduction CMOS Technologies Layout Design Rules – Technology - Related CAD Issues - Pitfalls and Fallacies - Historical Perspective Delay: Introduction - Definitions Timing Optimization - Transient Response

Unit III: Combinational Circuit and sequential circuit design [10 Hrs]

Combinational Circuit Design – Introduction - Circuit Families- Circuit Pitfalls - sequential circuit design Introduction Sequencing Static Circuits - Synchronizers

Unit IV: Datapath and Array Subsystems [11 Hrs]

Datapath Subsystems: Introduction - Addition/Subtraction - One/Zero Detectors - Array Subsystems: Introduction - SRAM - DRAM - Read-Only Memory - Serial Access Memories - Content-Addressable Memory - Programmable Logic Arrays

Unit V: Testing, Debugging, and Verification [10 Hrs]

Introduction - Testers, Test Fixtures, and Test Programs - Logic Verification Principles - Silicon Debug Principles - Manufacturing Test Principles - Design for Testability - Boundary Scan - Testing in a University Environment - Pitfalls and Fallacies

TEXT BOOKS:

1. Weste and Harris: CMOS VLSI DESIGN (Third edition) Pearson Education, 2005 (Unit I - V)
2. Uyemura J.P: Introduction to VLSI circuits and systems, Wiley 2002

REFERENCES:

1. D.A Pucknell & K.Eshraghian Basic VLSI Design, Third edition, PHI, 2003
2. Wayne Wolf, Modern VLSI design, Pearson Education, 2003
3. Randall .L.Geiger and P.E. Allen, " VLSI Design Techniques for Analog and Digital Circuits ", TATA McGraw-Hill International Company, 1990

SEMESTER – I
VLSI DESIGN USING VHDL
COURSE CODE: 14MEV104

Instructional hours per week: 5

Objective: To enable the students to learn the basic concepts of VHDL, different types of modeling and programming techniques using VHDL.

Unit I: Introduction to VHDL **[11 Hrs]**

Basic terminology – Design flow – VHDL objects – Entity declarations – Architectural body – Process declarations – Architectural body – Process declaration – Configuration – Functions – Procedures – Package declaration – Package body – Library

Unit II: Basic Language Elements **[10 Hrs]**

Identifiers – Data objects – Data types – Scalar – Real – Integer – Enumerators – Physical – Array – Composite – Operators – Logical – Relational – Shift – Adding – Multiplying – Miscellaneous

Unit III: Programming Model **[13 Hrs]**

Behavioral Modeling: Process Statement – Conditional Statement – IF, CASE, LOOP, NEXT and WAIT Statements, Assertion Statement – Exit Statement

Structural Modeling: Component declaration – Component instantiation – Signals – Variables – Delays – Inertial delay – Transport delay

Data Flow Modeling: Concurrent Statement – Concurrent versus Sequential Statement – Conditional Signal Assignment Statement

Unit IV: Model Simulation **[10 Hrs]**

Simulation – Writing a Test bench – Converting Real and Integer to Time – Dumping Results into a Text File – Reading Vectors from a Text File - A Test bench Example

Unit V: Applications **[11 Hrs]**

VHDL representation: Decoders – Encoders – Multiplexers – De-multiplexers – Adder – Subtractor – Multiplier – Counters – Shift registers – Simple ALU

TEXT BOOKS:

1. J. Bhasker, "VHDL Primer" III Edition, PHI, Six impression 2007

REFERENCE BOOKS:

1. Dougles L. Perry, "VHDL", III Edition, Tata McGraw Hill, 2002.
2. Moris Mano and Charles R. Kime, "Logic Circuit Layout and Design" II Edition, Pearson Education Asia, 2002

SEMESTER – I

PRACTICAL – I: VLSI SYSTEM DESIGN USING VHDL PROGRAMMING

COURSE CODE: 14MEV105

VLSI SYSTEM DESIGN USING VHDL PROGRAMMING

ANY TEN EXPERIMENTS:

1. Verification of logic gates with test bench
2. Generation of signals like sin, square, triangular wave with test bench
3. Four bit full adder and subtractor in single module wit test bench
4. Encoder and decoder with test bench
5. Multiplexer and demultiplexer with test bench
6. Flip flop and latches with test bench
7. Design a 2 bit Micro Processor with test bench
8. Memory Module both synchronous and asynchronous – RAM, ROM
9. Design a Finite state Machine and check the result with help of test bench
10. Design a Clock divider and generation
11. Interfacing of Seven Segment in Spartan 3 development kit
12. Interfacing of key board in Spartan 3 development
13. Interfacing of VGA in Spartan 3 development
14. Interfacing of UART in Spartan 3 development
15. Digital circuit design using Xilinx ISE

SEMESTER – I

PRACTICAL II: MICROCONTROLLER PROGRAMMING AND ITS APPLICATIONS

COURSE CODE: 14MEV106

Any Ten Experiments:

1. Arithmetic and Logic Operations
2. Data transfer with parallel port
3. Delay based on software and hardware timer
4. Object Counter
5. Interfacing Matrix Keypad
6. LCD interface
7. A/D interface
8. D/A interface
9. Seven Segment display interface
10. Traffic light controller
11. Water level controller
12. Stepper Motor Interface
13. Programmable timer
14. Serial interface
15. Digital clock

SEMESTER – II
VLSI DESIGN USING VERILOG
COURSE CODE: 14MEV201

Instructional hours per week: 5

Objectives: This paper enables the students to learn the statements, modeling structures and data types. It also motivates them to develop the programming skills to design a digital system.

Unit 1: Digital Design with Verilog HDL **[14 Hrs]**

Evolution of CAD - Emergence of HDLs, Typical HDL- based design flow, Trends in HDLs - Hierarchical Modeling Concepts - Design methodology-modules and instances-parts of a simulation - design block - stimulus block. Basic Concepts - Lexical conventions - data types - system tasks, compiler directives.- Modules and Ports- Module definition, port declaration, connecting ports, hierarchical name

Unit II: Gate level modeling & Data Flow Modeling **[11 Hrs]**

Gate-Level Modeling: Gate Types – Gate Delays – Examples, Dataflow Modeling: Continuous Assignments – Delays – Expressions, Operators and Operands – Operator Types. Examples

Unit III: Behavioral Modeling **[9 Hrs]**

Behavioral Modeling: Structured procedures- procedural assignments, Procedural - Assignments, Timing Control - Conditional statements - Multiway branching – Loops - sequential and parallel blocks - Tasks and Functions differences between tasks and functions - declaration, invocation - automatic tasks and functions. Examples

Unit IV: Advanced Verilog Topics **[10 Hrs]**

Advanced Verilog Topics: Timing and dalays-Types of delay models – path delay modeling – Timing Checks – Delay back annotation – Switch level modeling Elements – UDP basics – Combinational UDP Definition – Sequential UDP – UDP table shorthand symbols – Guidelines for UDP Design - Examples

Unit – V: Applications **[11 Hrs]**

FSM - Modeling Examples – Modeling Combinational Logic – Modeling sequential logic – modeling a memory – writing Boolean equations – Modeling a Ripple counter – Modeling a full adder with carry look ahead – Modeling a parameterized comparator – Modeling a decoder – Modeling a multiplexer

TEXT BOOKS:

1.Samir Planitkar "Verilog HDL" Second Edition IEEE 1364-20012 Compliant (Unit I - IV)

2.Douglas J Smith " HDL Chip Design" Doone Publications, Second Edition (Unit V)

REFERENCE BOOKS:

1. J.Bhasker, "Verilog HDL Synthesis, A Practical Primer", BS Publication, first Indian Edition, 2001 (Unit I, II, V)

2. Micheal D. Ciletti, "Advanced Digital Design with the Verilog HDL", PHI Publications, Indian reprint (Unit III, IV)

SEMESTER II

EMBEDDED SYSYEM & REAL TIMER OPERATING SYSTEM DESIGN

COURSE CODE: 14MEV202

Instructional hours per week: 5

Objective: To enable the students to understand the various Embedded Real time operating systems and to study the architecture of PIC microcontroller and also to develop application using embedded system.

Unit I: Embedded Software Architecture **[9 Hrs]**

Round Robin – Round Robin with Interrupts – Function Queue Scheduling Architecture – Real Time Operating Systems (RTOS) – Introductions to RTOS – Tasks and Data – Semaphores and Shared data

Unit II: Operating System Services **[11 Hrs]**

Message Queues, Mail box and Pipes – Timer Function – Events – Memory Management – Software Development Tools: Host and Target Machines – Linker\ Locaters for Embedded Software – Getting Embedded Software into target system

Unit III: Real time operating systems **[10 Hrs]**

VX works - µCOS – POSIX standards - Free RTOS - Salvo RTOS - Real time library of Keil IDE - RTOS Porting to a Target.

Unit IV: PIC CPU Architecture and Instruction Set **[15 Hrs]**

Overview – Harvard Architecture – Pipe lining – Program Memory considerations – Register like Structure and Addressing modes – CPU registers – Instruction Set – Simple Operations – External Interrupt and Timer - Overview RB0/INT External Interrupt Input Capture mode – Compare mode – Timer1/ CCP – Programming pre-scalar – Timer1 External Event counter – Timer1 and Sleep mode – PWM output – Port B Change Interrupts

Unit V: PIC Peripherals **[10 Hrs]**

Initialization and Programming of I2C bus for peripheral chip access – A/D Converters - UART – Serial Peripheral Interface – Special features.

TEXT BOOKS:

1. David E. Simon, "An Embedded Software Primer", Addison Wesley 2004 (Unit I & II)
2. John .B. Peatmen, "Design with PIC Microcontroller", Pearson Education, LPE, II reprint 2002 (Unit III, IV & V)
3. Micro µC OS II reference manual.
4. VX works Programmers manual.
5. Salvo OS Manual.

SEMESTER – II

ALGORITHM FOR VLSI DESIGN AUTOMATION

COURSE CODE: 14MEV203

Instructional hours per week: 5

Objective: This paper enables the students to analyze the circuits of hardware by software with an help of various algorithm.

Unit I: Design Methodologies **[11 Hrs]**

Introduction to VLSI design – Review of VLSI automation tools – Algorithmic graph theory and computational complexity – Tractable and intractable problem – General purpose methods for combinational optimization

Unit II: Selected Design problems and algorithm **[10 Hrs]**

Layout compaction – Design rules – Problem formulation – Algorithm for constraint graph compaction – Placement and partitioning – Circuit representation – Placement algorithm – partitioning

Unit III: Floor planning concepts **[11 Hrs]**

Floor planning concepts – Shape functional and floor sizing – Types for local routing problem – Area routing – Channel routing – Algorithm for global routing

Unit IV: Simulation **[11 Hrs]**

Simulation – Gate level modeling and simulation – Switch level modeling and simulation – Combinational logic synthesis – Binary decision diagrams – Two level logic synthesis

Unit V: High level synthesis **[12 Hrs]**

High level synthesis – Hardware models – Internal representation – Allocation – Assignment and scheduling algorithm – Assignment problem – High level transformation

TEXT BOOK:

1. Sabith H.Gerez, "Algorithms for VLSI Design Automation", John Wiley & Son, 1998 (Unit I - V)

REFERENCE BOOK:

1. Naveed A. Sherwani, Algorithm for VLSI Physical Design Automation Kluwer Academic Publications, 1999

2. Michael John Sebastian Smith. Application Specific Integrated Circuits, 1997

3. Baker, R. Jacob. CMOS Circuits Design, Layout and Simulation, IEEE Press New york.1997

SEMESTER – II

ELECTIVE – I: HIGH PERFORMANCE COMMUNICATION NETWORK

COURSE CODE: 14MEV203A

Instructional hours per week: 5

Objective: This paper enables the students to understand and to improve their practical knowledge in high performance communication networks.

UNIT – I: BASICS OF NETWORKS [12 Hrs]

Telephone, Computer, Cable Television And Wireless Network, Networking Principles, Digitalization – Service Integration, Network Services And Layered Architecture, Traffic Characterization And QOS, Network Services – Network Elements And Network Mechanisms

UNIT – II: PACKET SWITCHED NETWORKS [9 Hrs]

OSI and IP Models – Ethernet (IEEE 802.3), Token Ring (IEEE 802.5), FDDI, DQDB, and Frame Relay, SMDS – Internet Working With SMDS

UNIT – III: INTERNET AND TCP/IP NETWORKS [9 Hrs]

Overview – Internet Protocol – TCP And VDP – Performance Of TCP/IP Networks Circuit Switched Networks – SONET, DWDM, Fiber To Home, DSL, Intelligent Networks, CATV

UNIT – IV: ATM AND WIRELESS NETWORKS [12 Hrs]

Main Features – Addressing, Signaling And Routing, ATM Header Structure – Adaptation Layer, Management And Control BISDN, Interworking With ATM, Wireless Channel, Link Level Design, Channel Access, Network Design And Wireless Networks

UNIT – V: OPTICAL NETWORKS AND SWITCHING [13 Hrs]

Optical Links – WDM Systems, Cross-Connects, Optical LAN's, Optical Paths And Networks, TDS And SDS: Modular Switch Designs – Packet Switching, Distributed, Shard, Input And Output Buffers

TEXT BOOK:

1. Jean warland and pravin varaiya, "High performance communication networks", 2nd edition, Harcourt and Morgan Kauffman, London, 2000 (Unit I – V)

SEMESTER – II
ELECTIVE – I: ANALOG VLSI DESIGN
COURSE CODE: 14MEV203B

Instructional hours per week: 5

Objective: This paper enables the students to have basic knowledge about the analog VLSI and it also motivate them to develop the designing of Analog VLSI System

UNIT I: Basic CMOS Circuit Techniques, Continuous time and low voltage signal processing **[11 Hrs]**

Mixed – Signal VLSI Chips – Basic CMOS Circuits – Basic Gain Stage – Gain Boosting Techniques – Super MOS Transistor – Primitive Analog Cells – Linear Voltage – Current Converters – MOS Multipliers and Resistors – CMOS, Bipolar and Low – Voltage BiCMOS op-Amp Design – Instrumentation Amplifier Design – Low Voltage Filters.

UNIT II: Basic BICMOS circuit Techniques, current, Mode signal processing and Neural Information Processing **[11 Hrs]**

Continuous – Time Signal Processing – Sampled – Data Signal Processing - Switched – Current Data Converters – Practical Considerations in SI Circuits Biologically – Inspired Neural Networks – Floating – Gate, Low-Power Neural Networks – CMOS Technology and Models – Design Methodology – Networks – Contrast sensitive Silicon Retina.

UNIT III: Sampled Data Analog Fiiters, over filters, over sampled A/D converter Analog Integrated Sensors **[13 Hrs]**

First – order and Second SC Circuits – Bilinear Transformation – Cascade Design – Switched – Capacitor Ladder Filter – Synthesis of Switched – Current Filter – Nyquist rate A/D Converters – Modulators for Over sampled A/D Conversion – First and Second Order and Multibit Sigma – Delta Modulators – Interpolative Modulators – Cascaded Architecture – Decimation Filters – mechanical, Thermal, Humidity and Magnetic Sensors – Sensor Interfaces.

UNIT IV: Design for Testability and Analog VLSI interconnect **[10 Hrs]**

Fault modeling and Simulation – Testability – Analysis Technique – Ad Hoc Methods and General Guidelines – Scan Techniques – Boundary Scan – Built –in Self Test-Analog Test Buses – Design for Electron – Beam Testablity – Physics of Interconnects in VLSI – Scaling of Interconnects – A Model for Estimating Wiring Density – A Configurable Architecture for prototyping analog Circuits.

UNIT V: Statistical Modeling and Simulation, Analog Computer aided design and Analog and Mixed analog digital layout **[10 Hrs]**

Review of statistical Concepts – Statistical Device Modeling – Statistical Circuit Simulation – Automation Analog Circuit Design – automatic Analog Layout – CMOS Transistor Layout – Resistor Analog Circuit Design – automatic Analog Layout – CMOS Transistor Layout – Resistor Layout – Capacitor Layout – Analog Cell Layout – Mixed Analog – Digital Layout.

TEXT BOOKS:

1. Mohammed Ismail, Terri Fiez, "Analog VLSI signal and Information processing", Mc Graw-Hill International Editons (Unit I, II)
2. Malcom R.Haskard, Lan C.May," Analog VLSI Design – NMOS and CMOS", Prentice Hall (Unit III, IV)
3. Randall L Geiger, Phillip E.Allen, "Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company (Unit V)

SEMESTER – II

PRACTICAL – III: VLSI DESIGN USING VERILOG

COURSE CODE: 14MEV204

ANY TEN EXPERIMENTS:

1. Verification of logic gates with test bench
2. Generation of signals like sin, square, triangular wave with test bench
3. Four bit full adder and subtractor in single module wit test bench
4. Encoder and decoder with test bench
5. Multiplexer and demultiplexer with test bench
6. Flip flop and latches with test bench
7. Design a 2 bit Micro Processor with test bench
8. Memory Module both synchronous and asynchronous – RAM, ROM
9. Design a Finite state Machine and check the result with help of test bench
10. Design a synchronous and asynchronous Clock divider and generation
11. Interfacing of Seven Segment in Spartan 3 development kit
12. Interfacing of key board in Spartan 3 development
13. Interfacing of VGA in Spartan 3 development
14. Interfacing of UART in Spartan 3 development
15. Digital circuit design using Xilinx ISE Project Navigator

SEMESTER – II

PRACTICAL – IV: EMBEDDED SYSTEM & RTOS LAB

COURSE CODE: 14MEV205

ANY TEN EXPERIMENTS:

1) Parallel port interface
2) Delay generation using hardware timer
3) External event counter using timer 1
4) Internal ADC programming
5) Speed control of DC motor using PWM module
6) Interfacing RTC using I^2C bus
7) Interfacing serial EEPROM
8) UART interface
9) LCD interface
10) Temperature monitoring and control
11) D/A interface
12) Traffic Light controller
13) Water level controller
14) RTOS Multitasking
15) RTOS ISR
16) Priority Inversion

SEMESTER – II

SUPPORTIVE COURSE – I: ANALYSIS AND PROCESSING OF SIGNALS

COURSE CODE:

Instructional hours per week: 5

Objective: This paper enables the students to understand the basic concepts of signals and system and also to enable them to analyze various techniques like FFT, DFT and processing of audio / video signals.

UNIT – I: **[10 Hrs]**

An Introduction to DSP and its application – Signals – Requirements for linearity – static linearity and sinusoidal fidelity – Examples of linear and non linear systems – Special properties of linearity – Superposition, The foundation of DSP – Common decomposition – Alternative to linearity

UNIT – II: **[10 Hrs]**

The delta functions and impulse functions – Convolution – Mathematical properties of convolution – Correlation – Speed – The input side algorithm – The output side algorithm – The sum of weighted inputs

UNIT – III: **[10 Hrs]**

The family of Fourier transforms – Notation and formulated of the real DFT – DFT basic functions – Synthesis and analysis of DFT – Duality – Spectral analysis of signals – Frequency response of the systems – Convolution via the frequency domain

UNIT – IV: **[12 Hrs]**

How the FFT works – Speed and precision comparison – Continuous signal processing: The delta function – The convolution – The Fourier transform – The Fourier series

Introduction to digital filters – Filter basics – Time domain parameters – Frequency parameters – High pass filters – Band pass filters – Band pass and Band rejection filters

UNIT – V: **[13 Hrs]**

Audio processing – Human hearing – Timbre – Sound quality Vs Data rate – High fidelity audio – Compounding – Speech synthesis and Recognition – Image formulation and Display: Digital image structure – Cameras and End Eyes – Television video signals – Other image acquisition and display – Brightness and contrast adjustments – Warping

TEXT BOOK:

1. Steven. W. Smith, "The Scientist and Engineers guide to DSP", California Technical Publishing, California, 1999 (Unit I – V)

REFERENCE BOOKS:

1. S. Salivahanan, "Digital Signal Processing", TMH publish limited, New Delhi, 2008

2. John. G. Proakis and dimities G. Manolaks, "Digital Signal Processing", PHI Publications, 2003

SEMESTER – II

SUPPORTIVE COURSE – I: NEURAL NETWORK AND ITS APPLICATIONS

COURSE CODE:

Instructional hours per week: 5

Objective: This paper enables the students to have the basic concepts of neural networks and its applications.

UNIT – I: INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS [10 Hrs]

Neuro – Physiology – General Processing Element – ADALINE – LMS learning rule – MADALINE – MR2 Training Algorithm

UNIT – II: BPN AND BAM [14 Hrs]

Back Propagation Network – Updating of output and hidden layer weights – Application of BPN – Associative memory – Bi-directional Associative Memory – Hopfield memory – Traveling salesman problem

UNIT – III: SIMULATED ANNEALING AND CPN [10 Hrs]

Annealing, Boltzmann machine – Learning – Application – Counter Propagation network – Architecture – Training - Applications

UNIT – IV: SOM AND ART [10 Hrs]

Self Organizing map – Learning algorithm – Feature map classifier – Applications – Architecture of Adaptive Resonance Theory – Pattern matching in ART network

UNIT – V: NEOCOGNITRON [11 Hrs]

Architecture of Neocognitron – Data processing and performance of architecture of spacio – Temporal networks for speech recognition

TEXT BOOKS:

1. J.A. Freeman and B.M. Skapura, "Neural Networks, Algorithms Applications and Programming Techniques", Addision – Wesely, 1990
2. Laurene Fausett, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Prentice Hall, 1994

SEMESTER – II

SUPPORTIVE COURSE – I: ROBOTICS AND AUTOMATION

COURSE CODE:

Instructional hours per week: 5

Objective: This paper enrich the students and to understand the basic concepts of robotics organization and to develop new application using it.

UNIT – I: ROBOT ORGANIZATION [10 Hrs]

Coordinate transformation, Kinematics and inverse Kinematics, Trajectory planning and remote manipulation.

UNIT – II: ROBOT HARDWARE [13 Hrs]

Robot sensors – Proximity sensors – Range sensors – Visual sensors – Auditory sensors – Robot manipulators

Manipulator dynamics – Manipulator control – Wrists – End efforts – Robot grippers

UNIT – III: ROBOT AND ARTIFICIAL INTELLIGENCE [10 Hrs]

Principles of AI – Basics of learning – Planning movement – Basics of knowledge representations – Robot programming languages

UNIT – IV: ROBOTIC VISION SYSTEMS [11 Hrs]

Principles of edge detection – Determination optical flow and shape – Image segmentation – Pattern recognition – Model directed scene analysis

UNIT – V: ROBOT CONTROL AND APLLICATIONS [11 Hrs]

Robot control using voice and infrared – Overview of robot applications – Prosthetic devices – Robots in material handling, processing assembly and storage

TEXT BOOKS:

1. Vokopravotic, "Introduction to Robotics", Springer, 1988 (Unit – I)
2. Rathmill K., "Robot Technology and Application", Springer, 1985 (Unit – II)
3. Charniak & McDarmott, "Introduction to Artificial Intelligence", McGraw Hill, 1986 (Unit -III)
4. K.S.Fu, R.C.Gonzally, C.S.G.Lee, "Robotics Control, Sensing, Vision and Intelligence", McGraw Hill Book Company, 1997 (Unit – IV)
5. Mikell P. Groover, Mitchell Weiss, Roger. N, Nagel, Nicholas G. Odrey, "Industrial Robotic Technology Programming and Applications", McGraw Hill Book Company, 1986 (Unit – V)

SEMESTER – III
ASIC DESIGN
COURSE CODE: 14MEV301

Instructional hours per week: 5

Objective: To enable the students to learn about various types of ASIC, concepts and design flow of ASIC and to implement it with Micro wind software.

UNIT I: INTRODUCTION TO ASIC [10 Hrs]

ASIC Design – Introduction- ASIC Examples- Advantages – Types- Full custom ASIC, Semi – Custom ASIC – Standard cell – Based ASIC – GATE Array – based ASIC, -Channels gate array- Structured gate array – Field –Programmable Gate array- Programmable logic devices structure –PALs –PLDs – Programming of PALs – Field Programmable Gate array – ASIC design flow

UNIT II: PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS [12 Hrs]

Anti fuse- Static RAM- EPROM and EEPROM technology, PREP benchmarks - Actel ACT-Shannon's Expansion theorem - ACT2 and ACT3 logic module – Xilinx LCA – Altera FLEX – DC output – AC output - DC input - AC input - clock input- Power input – Xilinx I/O Block – Other I/O cells

UNIT III: PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY [10 Hrs]

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 –Altera MAX 9000 – Altera FLEX – Design systems – logic Synthesis – half gate ASIC - Schematic entry – Low level design language – PLA Tools – EDIF – CFI Design representation.

UNIT IV: ASIC CONSTRUCTION, FLOOR PLANNING [12 Hrs]

Physical Design- CAD tools - System partitioning – Estimating ASIC size –Power Dissipation – FPGA partitioning – Partitioning methods – Ratio cut algorithms – Look ahead algorithms - floor planning – Floor planning tools – I/O power Planning – Clock planning

UNIT V: PLACEMENT AND ROUTING [11 Hrs]

Placement –Measurement of placement – Placement algorithms – Simulated annealing – Timing driven Placement methods - physical design flow –Routing - global routing – detailed routing – special routing

TEXT BOOK:

1. M.J.S. Smith," Application – Specific integrated circuit" – Addison – Wesley Longman Inc, 2 reprint edition, 2000 (Unit I – V)

REFERENCE BOOKS:

1. Andrew Brown, "VLSI circuits and systems in silicon", Tata Mc Graw Hill Publications, 1991
2. S.D Brown, R.J.Francis, J.Rox , Z.G.Uransesic, " Field Programmable gate arrays" Khuever academic publisher, 1992
3. S.Y.Kung, H.J.Whilo House, T.Kailath, "VLSI and Modern Signal Processing" PHI Publications, 1985

SEMESTER – III
TI TMS 320C54X DSP
COURSE CODE: 14MEV302

Instructional hours per week: 5

Objective: To give an exposure to the fixed point TMS320C54X DSP architecture and to fulfill the specific needs of real time embedded applications using this processor.

UNIT I: [13 Hrs]

Introduction –TMS320DSP family overview-Applications for the TMS320DSPs-TMS320C54X DSP key features- Architecture Overview – Bus Structure- Internal Memory Organization – CPU – Pipeline Operation- Interrupt and the Pipeline – Dual access memory and pipeline

UNIT II: PROGRAM AND DATA MEMORY ADDRESSING [13 Hrs]

Immediate addressing – Absolute addressing – Accumulator addressing- Direct addressing – Indirect addressing – Memory mapped register addressing – Stack addressing – Data types – Program memory addressing

UNIT III: ON CHIP PERIPHERALS [10 Hrs]

Available on Chip peripherals – Peripheral memory mapped registers – General purpose I/O - timer – Clock generator – HPI

UNIT IV: SERIAL PORTS [9 Hrs]

Introduction – SPI – BSP – TDM

UNIT V: EXTERNAL BUS OPERATION [10 Hrs]

External Bus Interface – External Bus Priority- External bus control- External Bus Interface timing- Start up access sequence – Hold mode.

TEXT BOOK:

1. TMS 320C54X DSP reference set volume I: CPU and peripherals from Texas instruments (Unit I – V)

SEMESTER – III
ELECTIVE – II: ARM9 EMBEDDED PROCESSOR& RASPBERRY Pi
COURSE CODE: 14MEV303

Instructional hours per week: 5

Objective: To enable the students to understand & learn the architecture of ARM9 CPU with the Raspberry and explore their knowledge in embedded field.

UNIT – I: SAMSUNG S3C2440A ARM9 PRODUCT VIEW [13 Hrs]

Introduction – Features – Block diagram –Pin assignments – Signal Descriptions Programmers model – processor operating states – Switching state – Memory Format –Big and Little Indian – Instruction length – operating modes – Exceptions – Reset

UNIT – II: VARIOUS INTEGRATED CONTROLLERS [10Hrs]

Memory controllers: - Overview – functional descriptions – Nand Flash Controllers:- Features – Boot loader function – pin configuration – Nand Flash configuration table – Software modes – USB controllers

UNIT – III: PERIPHERAL INTEGRATION [10 Hrs]

Basic Timer: - Features – PWM Timer operation - I/O Port control description – Watchdog timer – Functional description of clock and Power management – DMA Operation – LCD Controller – STN LCD Controller operation – ADC and Touch screen interface operation

UNIT – IV: SERIAL INTERFACE [10 Hrs]

UART – Features – Block diagram and operation – MMC/SD/SDIO controller:- Features – Block diagram and SDIO Operation – IIC Bus interface – overview and operation – SPI – Features , Block diagram and operation- Camera Interface- AC97 Controller

UNIT – V: RASPBERRY PI & APPLICATION [12 Hrs]

Raspberry pi Setup and Management.- Operating system- software on raspberry pi – GPIO - Controlling of Hardware- Digital inputs – sensors – Displays

TEXT BOOK:

1. S3C2440A 32 bit CMOS Microcontroller user manual from Samsung (Unit I – IV)
2. Raspberry Pi Cookbook by Simon Monk, O'Reilly publication, December 2013 First Edition (Unit V)

SEMESTER – III
ELECTIVE – II: ANALYSIS AND DESIGN OF ANALOG IC's
COURSE CODE: 14MEV303A

Instructional hours per week: 5

Objective: To enable the students to learn about various analog ICs and to design applications using it

UNIT – I: CIRCUIT CONFIGURATION FOR LINEAR IC [13 Hrs]

Current sources, analysis of difference amplifiers with active load, supply and temperature independent biasing techniques, voltage references

UNIT – II: OPERATIONAL AMPLIFIERS [11 Hrs]

Analysis of Operational amplifier circuits, slew rate model and high frequency analysis, operational amplifier noise analysis and low noise operational amplifiers

UNIT – III: ANALOG MULTIPLIER AND PLL [11 Hrs]

Analysis of four quadrant and variable Tran conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL

UNIT – IV: MOS ANALOG ICs [10 Hrs]

Design of MOS Operational Amplifier, CMOS voltage references, MOS Power amplifier and analog switches

UNIT – V: MOS SWITCHED CAPACITOR FILTERS [10 Hrs]

Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC Filters.

TEXT BOOKS:

1. Gray and Meyer, "Analysis and Design of Analog ICs", Wiley International Publication, 1996 (Unit I, II)
2. Gray, Wooley, Brodersen, "Analog MOS Integrated Circuits", IEEE Press Publication, 1989 (Unit III)
3. Kenneth R. Laker, Willy M.C. Sansen, William M.C.Sansen, "Design of Analog Integrated Circuits and Systems", TATA McGraw Hill Publication, 1994 (Unit IV)
4. Behzad Razavi, "Principles of Data Conversion System Design", S. Chand & Company Ltd Publication, 2000 (Unit V)

SEMESTER – III

ELECTIVE – II: MOBILE COMPUTING
COURSE CODE: 14MEV303B

Instructional hours per week: 5

Objective: To enable the students to learn the basics of cellular concept, wireless LAN and wireless WAN.

UNIT I: WIRELESS COMMUNICATION SYSTEMS [11 Hrs]

Evolution of Mobile Radio Communication – Mobile Radio Telephony – Examples of Wireless Communication Systems – Trends in Cellular Radio and Personal Communication – Second Generation (2G) Cellular Networks – Third Generation (3G) Wireless Network

UNIT II: CELLULAR CONCEPT – SYSTEM DESIGN FUNDAMENTALS [10 Hrs]

Introduction – Frequency Reuse – Channel Assignment Strategies – Handoff Strategies – Interference and System Capacity – Trucking and Grade of Service

UNIT III: WIRELESS LAN [10 Hrs]

Infrared vs Radio Transmission – Infra Structure and Ad-Hoc Networks – IEEE 802.11 – HIPERLAN – BLUETOOTH – Mobile Transport Layer: - Traditional TCP – Classical TCP Improvements – TCP Over 2.513G Wireless Networks

UNIT IV: WIRELESS WAN [14 Hrs]

GSM and TDMA Technology – Introduction – What is GSM - Mechanism to Support a Mobile Environment – Communication in the Infra Structure.
CDMA Technology –Introduction – Reference – Mobile Data Network: - Introduction – The Data Oriented CDPD Network – GPRS and Higher Data Rates – Short Messaging Service in GSM – Mobile Application Protocol

UNIT V: WIRELESS NETWORKING [10 Hrs]

Introduction – Difference between Wireless and Fixed Telephone Network – Development of Wireless Networks – Fixed Network Transmission Hierarchy – Traffic Routing in Wireless Networks – Wireless Data Services – Common Channel Signaling – ISDN Signaling Systems

TEXT BOOKS:

1. Theodore S. Pappaport, "Wireless Communication Principles and Practice", PHI Publications, II Edition, 2005 ISBN-81-203-2381-5 (Unit I, II & III)

2. Jochen Schiller, "Mobile Communication", Pearson Education Second Edition ISBN-81-297-0350-5 (Unit IV & V)

REFERENCE BOOK:

1. Kaven Pahlavan Prashant Krishnamoorthy, "Principles of Wireless Networks" – PHI Publication, I Edition, 2002 ISBN-81-203-2380-7

SEMESTER – III
PRACTICAL – V: ADVANCED VLSI SYSTEM
COURSE CODE: 14MEV304

Any 10 Experiments:

IC LAYOUT DESIGN:

1. Study of Micro wind Layout design, Layer identification, Stick Diagram and DSRC

2. NMOS Transistor design/ PMOS Transistor design and Inverter Design

4. Serial in Serial out and Parallel in Parallel out register design

5. Sequential and Combinational Design

ALTERA FPGA IMPLEMENTATION:

7. LED and Seven Segment display interface

8. Alpha Numeric LCD Display Interface

9. UART Interface

10. Ps/2 Keyboard Interface

11. VGA Interface

SYSTEM VERILOG

12. Design and Verification of 4 bit full adder

13. Design and Verification of ALU

14. Design and Verification of RAM and ROM

15. Design and Verification of 2 bit Micro Processor

SEMESTER – III
PRACTICAL – VI: TI TMS 320C54X DSP
COURSE CODE: 14MEV305

Any 10 Experiments:

1. Generation of signals using MATLAB
2. Convolution of Discrete signals using MATLAB
3. Correlation of Discrete signals using MATLAB
4. FIR filter Design using MATLAB
5. IIR Filter Design using MATLAB
6. Generation of DFT and AM using MATLAB
7. Tone generation using PCM3002 codec module
8. Generation of ASK using TMS 320C5416 kit
9. Generation of FSK using TMS 320C5416 kit
10. Linear and Circular convolution using TMS 320C5416 kit
11. Generation of signals using TMS 320C5416 kit
12. Cross and Auto correlation using TMS 320C5416 kit
13. Interfacing A/D Converter
14. Object Counter using TMS320C5416 kit
15. Display blink using TMS320C5416 kit

SEMESTER - III

Supportive Course – II: System Verilog

COURSE CODE:

Instructional hours per week: 5

Objective: To enable the students to study the Digital system design using System Verilog and and to learn about the System Verilog is that it allows the user to construct reliable, repeatable verification environments

UNIT I: ADVANCED VERILOG [12 Hrs]

Verification of the gate level netlist –verilog coding style-deign partitioning-Example of circuit synthesis -Advanced verification techniques: Traditional verification flow-assertion checking-formal verification

UNIT II: INTRODUCTION AND DATA TYPE [10 Hrs]

The Verification Process - The Verification Methodology Manual - Basic Testbench Functionality - Directed Testing - Functional Coverage - Testbench Components – Data Types - Built-In Data Types – Fixed -Size Arrays- Dynamic Arrays- Queues - Associative Arrays- Linked Lists - Array Methods - Creating New Types with typedef - Creating User-Defined Structures - Type conversion - Enumerated Types – Constants – Strings

UNIT III: BASIC OOP [10 Hrs]

Introduction - OOP Terminology - Creating New Objects - Object Deallocation - Using Objects - Static Variables vs. Global Variables - Class Methods - Defining Methods Outside of the Class - Scoping Rules - Using One Class Inside Another - Understanding Dynamic Objects - Copying Objects - Public vs. Local - Straying Off Course - Building a Testbench

UNIT IV: INTERFACE AND RANDOMIZATION [10 Hrs]

Introduction - Ports - Interface Methods - Clocking Block - Virtual Interface - Overview - Random Variables - rand Modifier - randc Modifier - Constraint Blocks – External Constraint Blocks – Inheritance - if-else Constraints - Global Constraints - randomization Methods – randomize - pre_randomize and post_randomize - Inline Constraints - $rand_mode() - Disabling Constraints - $constraint_mode()- Random Number System Functions - $urandom - $urandom_range() - $srandom() - Random Stability

UNIT V: FUNCTIONAL COVERAGE [13 Hrs]

Coverage Types - Functional Coverage Strategies - Simple Functional Coverage Example - Anatomy of a Cover Group - Triggering a Cover Group - Data Sampling- Cross Coverage - Generic Cover Groups - Coverage Options - Analyzing Coverage Data - Measuring Coverage Statistics During Simulation – Conclusion

Text Books:

1. Verilog HDL A guide to Digital Design and Synthesis – Samir palnitkar (Unit I)
2. SystemVerilog for Verification, Second Edition -Chris Spear , Springer Publications (Unit II - V)
3. SystemVerilog 3.1 - Random Constraints – Proposal – Version by Synopsys

Reference Books:

A Practical Guide for SystemVerilog Assertions by Srikanth Vijayaraghavan Meyyappan Ramanathan , Springer Publications

SEMESTER – III

Supportive Course – II: DIGITAL IMAGE PROCESSING
COURSE CODE:

Instructional hours per week: 5

Objective: To enable the students to learn about images and systems and also to understand the concepts of image processing, restoration and compression techniques.

UNIT – I: CONTIUOUS AND DISCRETE IMAGES AND SYSTEMS [13 Hrs]

Light, Luminance, Brightness and Contrast, Eye, The Monochrome Vision Model, Image Processing Problems and Applications, Vision Camera, Digital Processing System, 2-D Sampling Theory, Aliasing, Image Quantization, Lloyd Max Quantizer, Dither, Color Images, Linear Systems And Shift Invariance, Fourier Transform, Z-Transform, Matrix Theory Results, Block Matrices and Kronecker Products.

UNIT – II: IMAGE TRANSFORMS [8 Hrs]

2-D orthogonal and Unitary transforms, 1-D and 2-D DFT, Cosine, Sine, Walsh, Hadamard, Haar, Slant, Karhunen-loeve, Singular value Decomposition transforms.

UNIT – III: IMAGE ENHANCEMENT [13 Hrs]

Point operations - contrast stretching, clipping and thresholding density slicing, Histogram equalization, modification and specification, spatial operations - spatial averaging, low pass, high pass, band pass filtering, direction smoothing, medium filtering, generalized cepstrum and homomorphic filtering, edge enhancement using 2-D IIR and FIR filters, color image enhancement.

UNIT – IV: IMAGE RESTORATION [8 Hrs]

Image observation models, sources of degradation, inverse and Wiener filtering, geometric mean filter, non linear filters, smoothing splines and interpolation, constrained least squares restoration.

UNIT – V: IMAGE DATA COMPRESSION AND IMAGE RECONSTRUCTION FROM PROJECTIONS [13 Hrs]

Image data rates, pixel coding, predictive techniques transform coding and vector DPCM, Block truncation coding, wavelet transform coding of images, color image coding. Random transform, back projection operator, inverse random transform, back projection algorithm, fan beam and algebraic restoration techniques.

TEXT BOOKS:

1. Anil K.Jain, "Fundamentals of Digital Image Processing", PHI Publications, 1995 (Unit I, II, III)
2. M.A.Sid Ahmed,"Image Processing", TATA McGraw Hill Publications, Inc, 1995 (Unit IV, V)

REFERENCES BOOKS:

1. R.Gonzalaz and E. Woods, "Digital Image Processing", Addison Wesley Publications, II Edition, 1987
2. William. K.Pratt, "Digital Image Processing", Wiley Interscience Publications, II Edition, 1991

tion, 1991

SEMESTER – III

Supportive Course – II: MULTIMEDIA COMPRESSION TECHNIQUES

COURSE CODE:

Instructional hours per week: 5

Objective: To enable the students to understand the concept of compression techniques in multimedia and various protocols in multimedia.

UNIT – I: INTRODUCTION [13 Hrs]

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video

UNIT – II: SUBNETWORK TECHNOLOGY [12 Hrs]

Broadband services, ATM and IP, IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance

UNIT – III: MULTICAST AND TRANSPORT PROTOCOL [10 Hrs]

Multicast over shared media network, multicast routing and addressing, scalping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP

UNIT – IV: MEDIA - ON – DEMAND [10 Hrs]

Storage and media servers, voice and video over IP, MPEG-2 over ATM/IP, indexing synchronization of requests, recording and remote control

UNIT – V: APPLICATIONS [10 Hrs]

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy

TEXT BOOKS:

1. Jon Crowcroft, Mark Handley, Ian Wakeman, "Internetworking Multimedia", Harcourt Asia Pvt.Ltd. Singapore, 1998 (Unit I, II)

2. Tay Vaughan, "Multimedia making it to work", TATA McGraw Hill Publication, IV Edition, 2000 (Unit III, IV, V)

SEMESTER – IV
MEMS AND NEMS
COURSE CODE:14MEV401

Instructional hours per week: 5

Objective: To enable the students to learn about various materials used in MEMS and NEMS. Also to study the operation of various MEMS sensors and their fabrication process

UNIT I: OVERVIEW OF MEMS AND WORKING PRINCIPLES OF MICROSYSTEM [15 Hrs]

Mems as Micro sensor-Micro actuator- Microsystems products –Comparison of Microsystems and Microelectronics – Multi disciplinary nature of Microsystems design and manufacturing – Applications of Microsystems

Micro sensors: Bio medical and Biosensor– Chemical Sensor – Thermal sensor

Micro Actuation: Actuation by Thermal Forces, Shape Memory Alloys, Piezo Electric Crystals and Electrostatic Force-Micro motors –Micro valves – Micro pumps- Micro Accelerometer

UNIT II: MATERIALS FOR MEMS [10 Hrs]

Substrates And Wafer – Czochralski method for growing single crystal- Crystal structure– Silicon Compounds – Silicon Dioxide – Silicon Carbide –Silicon Nitride – Poly Crystalline Silicon-Polymers –The Longmuir Blodgett (LB) Film

UNIT III: MICROSYSTEM FABRICATION PROCESS [10 Hrs]

Photolithography – Ion Implantation – Diffusion – Oxidation –CVD-PVD– Sputtering – Deposition by Epitaxy – Etching

UNIT IV: MICROMANUFACTURING AND MICRO SYSTEM DESIGN [10 Hrs]

Micro Manufacturing: Bulk Micro Manufacturing – Surface Micro Machining – The LIGA process

Microsystems Design **:** Design consideration –Computer Aided Design (CAD)

UNIT V: NEMS PROPERTIES AND APPLICATION [10 Hrs]

Properties of Nano material: Mechanical properties-Melting of Nano particles- Electrical conductivity-Optical properties

Applications: Electronics- Automobiles-Domestic appliances-Bio-technology and Medical field-Space and Defense.

TEXT BOOKS:

1. Tai – Ran Hsu, " MEMS and Microsystems Design and Manufacture " Tata McGraw Hill Edition 2002, ISBN 0 – 07-048709- X (Unit I – IV)

2. Sulabha K. Kulkarni, " Nano technology: principles and practices" Capital publishing company (Unit V)

3. P.K. Sharma, "Understanding Nano Technology", Vista Publications, I Edition, 2008 (Unit V)

SEMESTER – IV
AUTOMOTIVE EMBEDDED SYSTEMS
COURSE CODE: 14MEV402

Instructional hours per week: 5

Objective: To enable the students to understand the various architecture and technologies used in automotive vehicles. It also helps them to learn the embedded communications used in Automotives.

UNIT-I: AUTOMOTIVE ARCHITECTURE [11 Hrs]

General Context - Functional domains-Standardized components, Models and Processes – Certification Issue of safety critical In Vehicle embedded systems

UNIT-II: INTELLIGENT VEHICLE TECHNOLOGIES [10 Hrs]

Road transport and its evolution – New technologies – Dependability Issues – Autonomous Car

UNIT-III: AUTOMOTIVE PROTOCOLS [10 Hrs]

Automotive communication Systems Characteristics and constraints – InCar Embedded Networks – Middleware Layer – Open issues for Automotive Communication Systems

UNIT-IV: EMBEDDED COMMUNICATIONS [15 Hrs]

FLEX RAY

Introduction - Event driven verses Time driven communication-Objectives of flex ray-Flex ray communication-Frame format -Communication cycle-Static segment-Dynamic segment

FLEX CAN

Main requirements of Automotive Networking - Network technologies- CAN features and limitations-Control system - Flex CAN architecture-Flex CAN address CAN limitations- Flex CAN applications

UNIT – V EMBEDDED SOFTWARE: **[9 Hrs]**

Product Lines in Automotive Electronics

Characteristics of Automotive Product Lines – Basic Technology – Global Coordination of Automotive Product line variability – Artifact level variability

TEXT BOOK:

1. NICOLAS NAVET, FRANCAISE SIMONOT –LION, "Automotive Embedded Systems Hand Book" , CRC Press (Unit I – V)